ECHO CANCELLATION

ON COMMUNICATION CIRCUITS

A thesis presented for the degree of
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by

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ABSTRACT

Echoes present on telephone circuits are a significant problem on long circuits where the round trip delay is greater than 100 mS. This is particularly so on satellite circuits where the round trip delay is in the order of 500 mS for each satellite hop.

An echo canceller has been designed for New Zealand conditions which is less complex and, therefore, should be less expensive to produce than current overseas models. Although particularly applicable to New Zealand conditions, the techniques used have wider application. The general problems of echo canceller design are considered with some specific proposals being made.

The two cancellers described here are non-adaptive and are based on a digital transversal filter. The later canceller employs Random Access Memory (RAM), uses pseudo random noise for system identification and compands the speech samples and filter coefficients in a true logarithmic format using multiplexing. techniques for bulky and costly components.

ACKNOWLEDGEMENTS

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I am also grateful to Professor R.H.T. Bates and Dr J. H. Andreae for their guidance, interest and critical appraisal of my work.

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I wish also to thank my wife Judy for her encouragement and patience in the frustration of being unable to fully understand the details of the project.

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GLOSSARY

A/D	analogue to digital conversion
D/A	digital to analogue conversion
ERLE	echo return loss enhancement - defined as the ratio of the echo at the input of transmit path of echo canceller and the residual echo appearing at the output of the transmit path
ETA	echo transfer attenuation - defined as the ratio of the signal on the receive path (relative to traffic level) causing the echo to the echo on the transmit path (relative to traffic level)
PCM	pulse code modulation
RAM	random access memory - solid state memory in this context
PROM	programmable read only memory - solid state memory in this context
PRBS	pseudo random binary sequence
DFT	discrete fourier transform
FFT	fast fourier transform
h(kT)	discrete impulse response of the echo path
e(kT)	discrete samples of the true echo
e'(kT)	discrete estimate of the echo
r(kT)	discrete response of the echo path
n(kT)	discrete samples of noise appearing as an echo

$s(kT)$	discrete samples of the signal leaving the canceller for the near end subscriber - is used to represent either speech or transmitted noise
$s'(kT)$	extended version of the transmitted noise sequence
$\psi_{s'r}(kT)$	discrete correlation of the response of the echo path with the extended noise sequence
$\psi_{s's}(kT)$	discrete correlation of the extended noise sequence with the sequence itself
$\psi_{s'n}(kT)$	discrete correlation of the extended noise sequence with the noise on the echo path
$\psi_{sr}(kT)$	discrete correlation of the transmitted noise sequence with the response of the echo path to that sequence
$\psi_{ss}(kT)$	discrete auto-correlation of the transmitted sequence
σ	standard deviation of a distribution
dBm	level in dB relative to 1 milliwatt in 600Ω
dBmO	level in dB relative to the R.M.S. value of the maximum amplitude signal to be carried without clipping
2W	2 - wire
4W	4 - wire
Tx	transmit
Rx	receive

PREFACE

Echoes have always been present on national telephone circuits due to the mismatch between local and national circuits. For calls internal to a country, the round trip delay for echoes is normally so short that the echoes are not perceived as such. With international calls and especially those via satellite, the delay is such that the echoes are clearly detectable.

Advances in technology, especially over the last decade, have enabled new solutions to be found to this problem which has traditionally been handled with echo suppressors. Echo cancellation refers to the generation of an estimate of the expected echo, which is then used to cancel out the actual echo received. Echo suppressors rely on the introduction of loss into the return path to attenuate the echo.

This thesis is primarily concerned with the development of an echo canceller designed specifically for New Zealand conditions, which should be economically competitive with the traditional suppressor. Until now cancellers developed for and by other countries have been relatively complex and expensive, due partly to the conditions they have been required to meet. A

simpler and consequently less expensive model is presented which while meeting New Zealand requirements could also be adapted to similar situations overseas.

This thesis describes two cancellers. The first is an initial attempt to provide a simple and inexpensive unit. It is felt that this was a necessary and important step in the evolution of the later design. In itself it had certain inherent disadvantages but provided a background on which the later model was developed. This later model overcame the now obvious shortcomings of the first canceller and uses techniques not previously applied to the echo cancellation field. Other proposals are made which are not included in this design but are applicable to problems experienced outside New Zealand. The use of true logarithmic compression of speech and filter coefficients, pseudo random noise testing of the echo path and the application of the Hilbert Transform are among these. New material and applications are included in Chapters 2-7.

In Chapter 1 an introduction is given to the reasons for echoes on communication circuits and their characteristics. A summary of echo suppressor and echo canceller developments and a critical appraisal of their relative merits are given with an explanation of the reasons for, and the direction of my research. The possibility of applying modern echo cancellation techniques to artificially enhance the acoustics of an auditorium is also briefly discussed.

In Chapter 2 the first prototype canceller is described and the results of tests are given. The shortcomings are described. This canceller was an introduction to this field of research for the author. Attempts to simplify certain aspects in fact resulted in some undesirable complexities. The use of Random Access Memory proved convenient but the principle of analogue gain adjustment around the digital processing section might have been a source of difficulty in an operational situation. The policy of single impulse testing of the echo path, although attractive for its simplicity, could have proved ineffective without some form of averaging.

In Chapter 3 the primary problem in echo canceller design is studied. Problems with the method for establishing the filter coefficients in the first canceller are explained. The development of a modified version of the widely used psuedo random binary sequence is explained as a suitable method of averaging out the noise contribution to errors in measuring the impulse response. Reasons are given for the choice of this method of obtaining the filter coefficients over the widely accepted practice of allowing coefficients to adapt or converge to their correct value.

In Chapter 4 true logarithmic companding is proposed as a suitable format for the storage and processing of speech samples and filter coefficients. The conversion from a 12 bit linear format to an 8 bit logarithmic format not only reduces storage but drastically simplifies the convolution process. The suitable choice of a logarithmic base is explained along with the dynamic range considerations and the problem of taking logarithms near zero.

In Chapter 5 the complications of time variance of echo path characteristics are discussed. A new method of tracking cyclic time variance is proposed which uses the predictability of this form of time variance to advantage. This problem severely restricts the performance of the normal adaptive canceller where it occurs. The problem had not previously been attacked in this manner.

In Chapter 6 the Hilbert Transform is proposed as a means of generating a quadrature component of the echo estimate. The use of discrete convolution in the time domain to generate this quadrature component, enables the application of any phase shift, by the correct combination of the real and quadrature components. A constant variation of this phase per unit time results in a frequency shift or phase roll.

In Chapter 7 the design of the echo canceller based on the previously developed principles is discussed. A multiplexed system is shown which is very cost effective on a per channel basis, with most expensive components including coefficient measuring circuitry being time shared over many circuits. Results of interim tests on this coefficient measuring circuitry are given but cancellation tests are not completed.

In Chapter 8 a summary of the project is given in light of the prescribed aims. A section headed 'Hindsight' lists some of the errors of judgement and misdirected effort which are more easily recognised afterwards. The future of the project is considered as it becomes the responsibility of the Post Office.

Papers completed to date on topics related to this thesis are as follows:

Webb, Joseph A. and Kelly, M. W., "Telephone Echo Cancellation for Satellite Terminals" IEEE Conf. Proc., ICC'78, Vol. 1, pp. 10.5.1 - 10.5.5.

Webb, Joseph A. and Kelly, M. W. "Delay Lines help generate Quadrature Voice for SSB" Electronics, April 1978, pp. 115 - 117.

Webb, Joseph A. and Kelly, M. W., "An Improved Echo Cancellation Technique" 1979, paper resubmitted to IEEE Trans. Commun. as requested by assessors.

Webb, Joseph A. and Kelly, M. W. "Practical Sampling Considerations" 1979, paper resubmitted to IEEE Trans. Commun. following request for further information.

Reprints of these papers can be found in Appendix I.

CHAPTER ONE

REVIEW OF ECHO SUPPRESSION AND CANCELLATION

1.1 INTRODUCTION

The presence of echoes on telephone circuits causes difficulty in communication where the round trip delay of the echo is long. This is the case with international circuits, especially where satellite circuits are encountered. The traditional method of reducing the level of echoes on telephone circuits has been to use echo suppressors. Suppressors have not been entirely satisfactory, especially where satellite circuits are involved, and the delay is excessive.

With advances in modern technology, echo cancellation as a means of reducing echo levels has received a lot of attention. The causes of echoes, and the development of both suppressors and cancellers to control the problem, are explained in this chapter.

A mention is also made of the application of the signal processing techniques used in echo canceller design to the processing of echoes in an auditorium.

1.2 ECHOES ON TELEPHONE CIRCUITS

The telephone network in any country comprises two types of circuit:

(i) The local circuit connecting the subscriber to his local telephone exchange, which comprises one bi-directional circuit, normally of one pair of wires. This circuit is termed a 2-wire (2W) circuit.

(ii) The national circuit, which connects exchanges throughout the country on various types of transmission systems, comprises two uni-directional circuits and is often called a 4-wire (4W) circuit with separate send and receive paths.

1.2.1 How Echoes Occur

It is at the junction of the local and national circuits that echoes are assumed to be generated. Although this is not strictly true, as echoes can originate at any mismatch in the 2W circuit, it is a convenient and safe assumption. At this junction is the Hybrid Transformer 2-wire to 4-wire interface circuit, which ideally passes all incoming speech from the national circuit out to the local circuit without passing any of this energy back on to the outgoing side of the national circuit. However, these units are never perfect and are seldom adequate. As these transformers are permanently associated with the national circuit, any local circuit may be connected to them, all of which will present a different load to the 2W connection on the Hybrid. A diagram showing a national telephone circuit can be seen in Fig. 1.1. With a varying load on the Hybrid Transformer it cannot be satisfactorily adjusted (balanced) to suit all circuits, and the relatively high levels of leakage result in echoes. Although reflections at the subscriber's end of the local circuit are present, these

are of lower amplitude, with the hybrid leakage, therefore, normally being the major contributor.

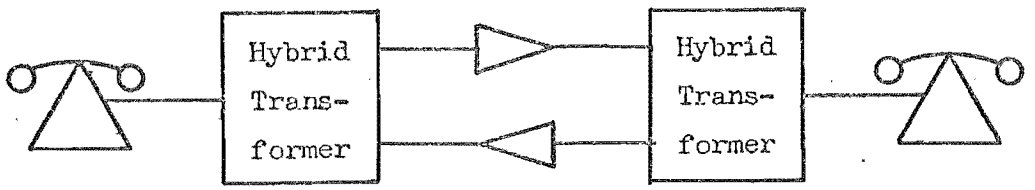


Fig. 1.1 National Telephone Circuit

Although a typical attenuation figure for the leakage path is 20 dB, the relative level of send and receive on the 4W connections to the hybrid is such that the echo is much less than 20 dB below the outgoing speech. These levels are shown in a diagram of the Hybrid in Fig. 1.2.

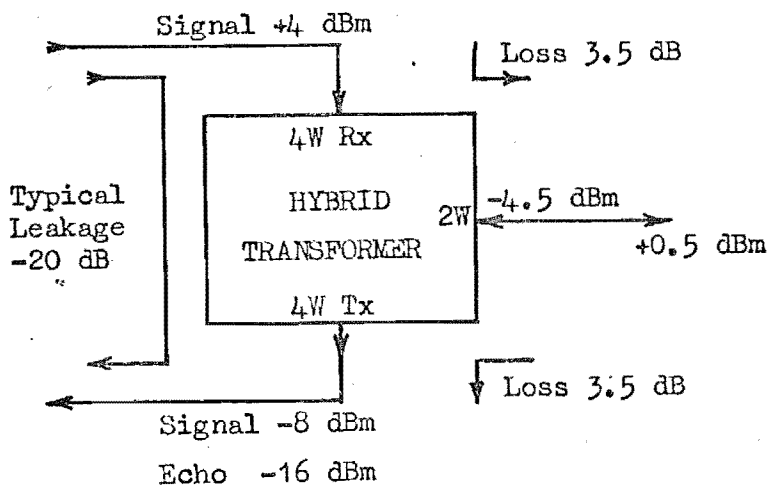


Fig. 1.2 Hybrid Transformer Levels

It is, therefore, apparent that to some extent echoes will be present on all calls on the national network due to the imperfect nature of the match between local and national circuits.

1.2.2 Characteristics of the Echo Path

Many tests have been carried out on national telephone networks to establish the characteristics of the echoes encountered by subscribers. Results of tests on the French network and the American network have been published by CCITT[12] and Duffy[37] respectively. These results give a good basis for establishing echo characteristics. Levels of echo are given by the Echo Transfer Attenuation (E.T.A.), being defined as the relative level of the echo on the send path, to the signal producing the echo on the receive path, where both paths are at the same nominal traffic level. This figure, therefore, takes account of the different levels for each path at the hybrid and gives a true indication of the level of the echo relative to the speech generating it. Results from tests on the French network, published by CCITT[12], give a mean E.T.A. of 13.6 dB with a standard deviation of 5.1 dB. A histogram showing distribution of E.T.A.s is reproduced from the CCITT report in Fig. 1.3.

This means that the echo is typically only 13.6 dB below the incoming speech. This, however, is not a problem on National networks as the round trip delay for the echo is typically less than 32 mS according to test results already mentioned. For delays of this order, the echo is

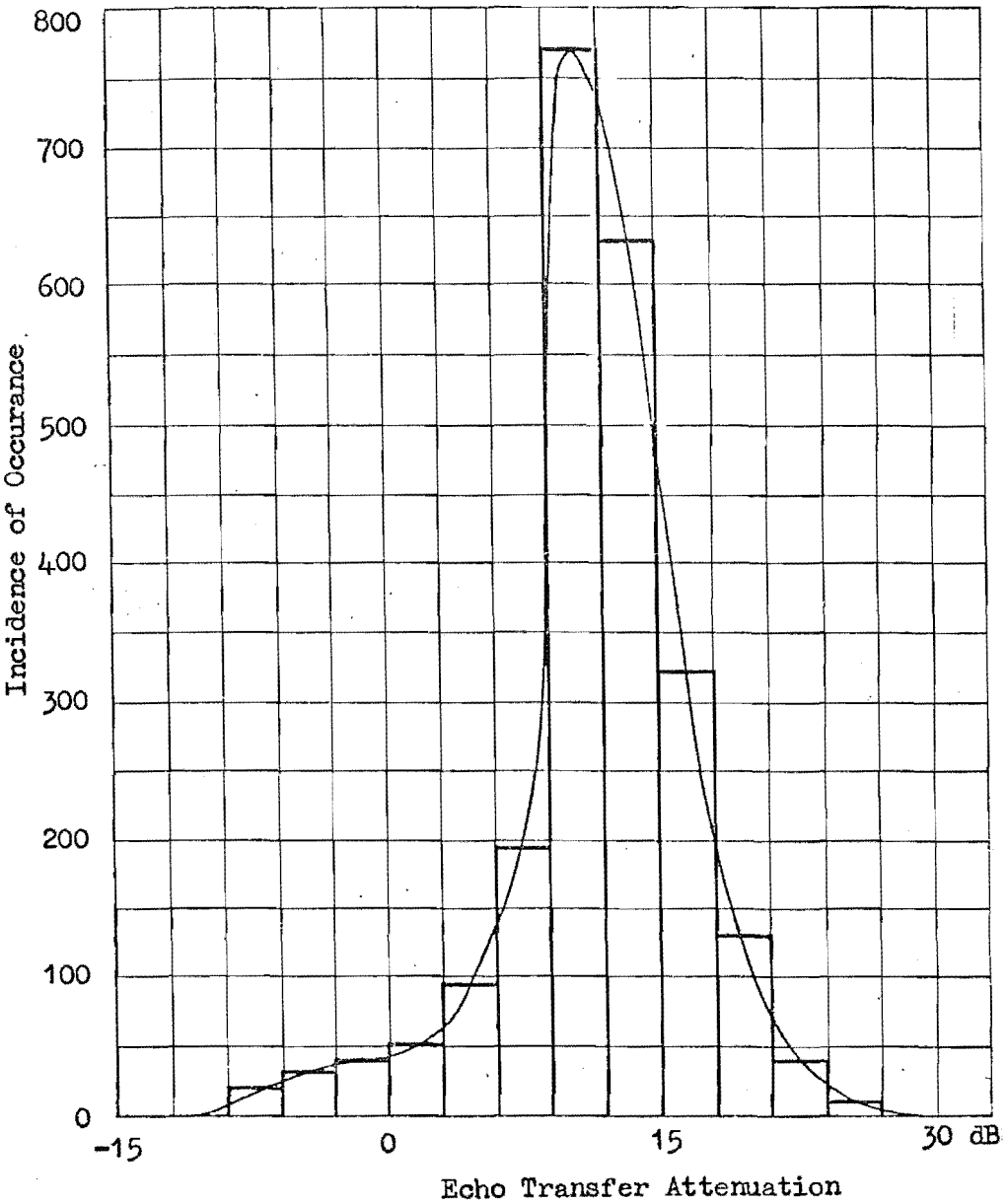
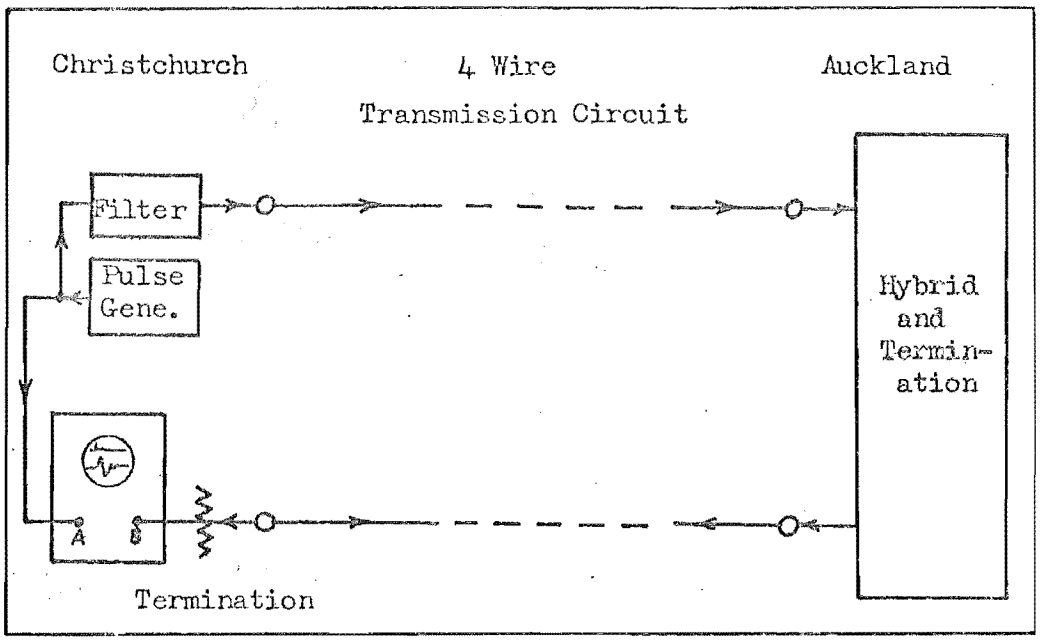


Fig. 1.3 Histogram of Echo Transfer Attenuation Distribution. Reproduced from Ref. (12)

not perceived as an echo and appears as sidetone to the subscriber.

The other characteristic of interest in echo canceller design is the pattern of the impulse response of the echo path and its energy distribution. The above tests established that the maximum length of the impulse response to the end of the active period was 32 mS. This may not be true of larger countries but is true of the New Zealand network. The impulse response comprises a delay portion where no activity is present, and then an active period where 99% of all energy is found in a period of 8 mS. To verify that these characteristics were also typical of the New Zealand network some impulse response measurements were made between Christchurch and Auckland, a distance of approximately 550 miles. An initial delay period of 11 mS, with an active period of 8 mS, was typical. As the distance between Christchurch and Auckland is two thirds of the maximum circuit length in New Zealand, a 32 mS impulse response would not be exceeded on the New Zealand network. A group of typical impulse responses obtained are shown in Fig. 1.4, along with the test circuit used.

Time variance of the echo path is another important consideration. Intermittent variations in the echo path can be caused by circuit switching or subscriber switching. Cyclic time variance is caused by a frequency shift around the echo path, due to non-synchronised oscillators in a Frequency Division Multiplexed system. This causes the phase of the impulse response to vary continuously at up to about 15 rad/sec in some networks. A more detailed



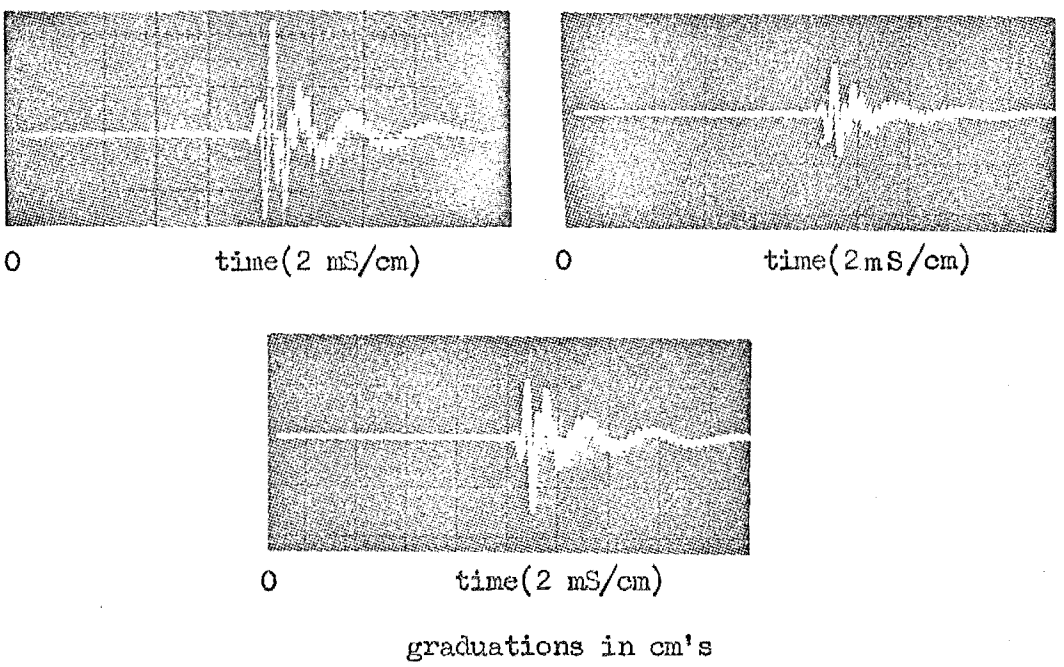


Fig. 1.4 Test Setup and Typical Impulse Responses for Auckland-Christchurch Toll Circuit

explanation of this phenomena is given in Chapter 5. Results of tests on the Australian network[28] have shown that 6.6% of all subscribers will encounter a circuit with phase roll on an international call, with a further 8.2% possibly encountering one. Of these subscribers, 30% will encounter phase roll greater than 0.5 Hz, with a maximum rate of phase roll at 5 Hz.

1.2.3 The Effect of Delay on Speech Communication.

There are two distinct effects of delay on the communication between two subscribers on a telephone circuit. The first is the effect of having to wait longer than normal for a reply. This effect causes no difficulty until the delay exceeds 50 milliseconds. The second is the effect that this delay has on echoes, which would otherwise provide no difficulty. The combination of these effects causes confusion and considerable difficulty as the delay increases. Subjective tests have been carried out by CCITT[20] to ascertain the relationship between echo level, round trip delay and difficulty experienced. A graph showing these relationships is given in Fig. 1.5, having been reproduced from this report.

These difficulties are experienced to some extent in larger countries on national calls, but only where the round trip delay exceeds about 50 mS. Otherwise national toll networks do not experience these difficulties in the case of internal calls.

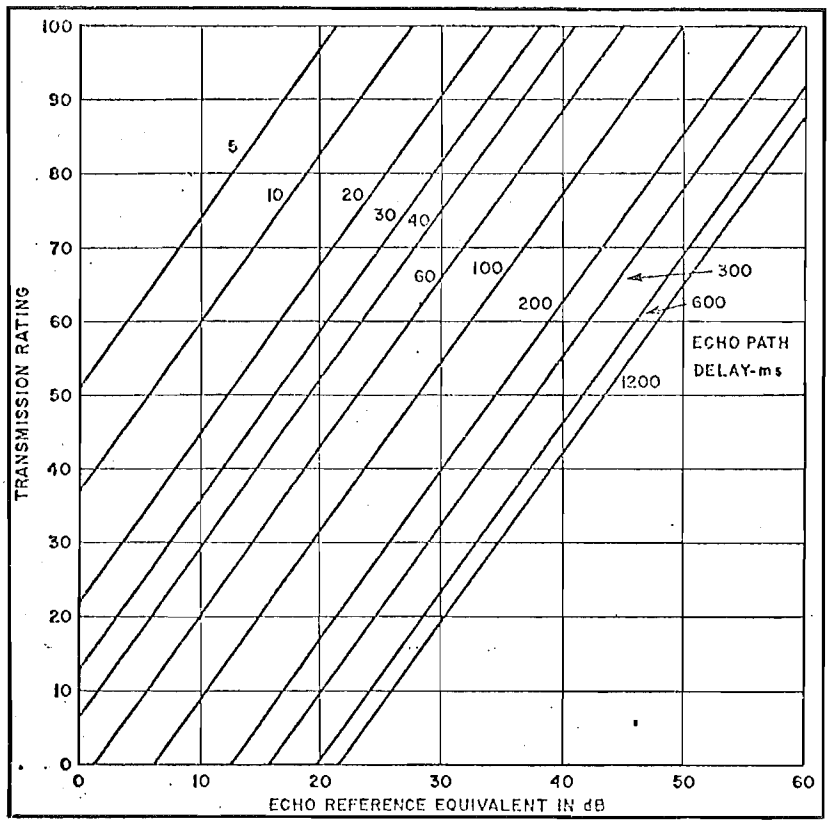


Fig. 1.5 Transmission rating vs Delay in Telephone Network. Reproduced from Ref. (20)

On international telephone connections, however, the problem affects all countries. This is especially so where international connections are made via satellite. The physical length of the round trip path in this case becomes much greater than is the case for cable circuits. This results in a significantly increased delay for echoes. An illustration of the path lengths and subsequent delays is shown in Fig. 1.6. With satellites being at an altitude of around 36,000 km, a minimum round trip delay of 500 mS for each satellite 'hop' is introduced. With this delay an echo is clearly perceptible, and for this reason the incorporation of more than one satellite hop in a telephone circuit is avoided whenever possible. For video and other

transmissions, no such limitation applies.

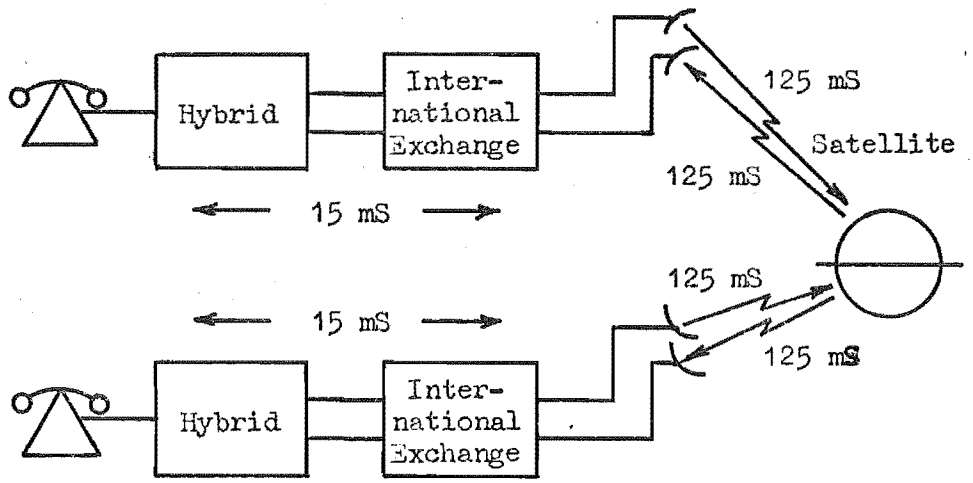


Fig. 1.6 Delays caused by satellite circuits

An interesting side effect of this confusion, caused by the presence of an echo, is the difficulty in speaking without stuttering. Gould & Helder[45] suggest that the annoyance could be due to the dislike of being mimicked. Tiffany & Hanley[83] have used delayed echoes as a means of determining a person's ability to hear, by that person's ability to talk without stuttering in the presence of echoes.

Another variable studied recently by CCITT[25] is that of frequencies which are most annoying in the echo. It was found that a narrow bandwidth of echo between 500 Hz and 1 kHz was most easily detectable, with echoes being equally detectable at 250 Hz and 2 kHz needing to be 10 dB higher. Although this knowledge is of no obvious benefit, it is possible that echo control device design could benefit from this knowledge. Specifically, the device could be

designed so as to more accurately suppress these frequencies at the expense of others.

Although echoes are a major contributor to conversational difficulties, the confusion caused by the delay alone is significant. This problem has been widely studied and the effects published. Richards[75] has been a major contributor in this area.

1.3 ECHO CONTROL ON COMMUNICATION CIRCUITS

There are two main methods of reducing echo levels on telephone circuits:

(1) Echo Suppression

(2) Echo Cancellation

Echo suppression refers to the practice of inserting a fixed amount of attenuation - normally 50 dB - into the return path, to prevent the echo being retransmitted to the distant subscriber. Echo cancellation involves no such interruption to the path but relies on the generation of a second echo by a filter, which is then used to cancel out the genuine echo. Ideally the filter represents an accurate model of the true echo path, and the cancellation by subtraction is perfect.

1.3.1 Echo Suppression

Echo suppressors are the traditional method of reducing echoes, and they have proved quite satisfactory prior to the advent of satellite circuits for telephone connections. The principle of suppressors is to attenuate

the echo on its return path. A control circuit determines when the distant subscriber only is talking, and inserts 50 dB of attenuation into the return path. When the near subscriber talks - even during the time when both are talking - the attenuation is removed. A schematic diagram of this process is shown in Fig. 1.7.

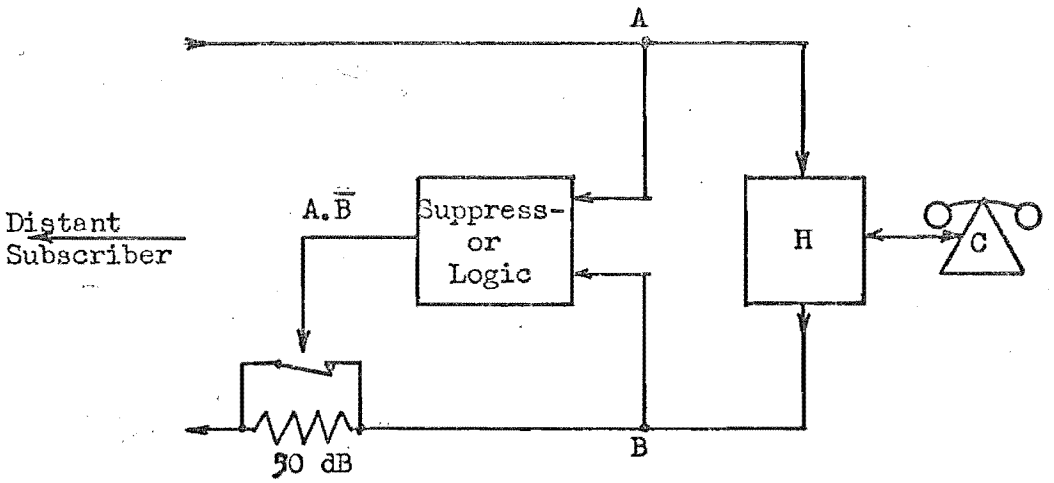


Fig. 1.7 Echo Suppressor Operation

Practically some difficulty is experienced in determining whether speech present at 'B' is due to 'C' or an echo from 'A'. If the decision was made as shown in the simple diagram above, an echo present due to 'A' would appear as speech from 'C' and the suppressor would never operate. A decision must, therefore, be made as to the origin of the energy. The ever present conflict of cost versus performance means that wrong decisions are invariably made at times by the circuitry. These mistakes increase as delay and confusion increase the instances of double talking, i.e. when both parties talk together. These wrong decisions cause attenuation of the wanted speech signals, this being termed 'chopping'. The problem of determining

which signals are echoes has been studied widely by many people including Unrue[85].

Specifications quoted by S.T.C. for their echo suppressor models SP-10 and SP-20 give an example of the characteristics of modern suppressors. These suppressors insert a 60 dB loss in the transmit path when incoming speech only is present. When both transmit and receive paths are in use, the 'break-in' circuit inhibiting suppressor operation comes in when the transmit signal level is higher than the receive level. During this time a 6 dB pad is inserted in the receive path. This same inhibited operation occurs when speech is only present on the transmit path. Those performance specifications of particular interest are:

Operate times:	Suppression: <5 mS
	Break-in: <30 mS (receive level constant) - typically 20 mS
Hangover times:	Suppression: 40-75 mS
	(typically 50-60 mS)
	Break-in: 150-350 mS
	(typically 200-300 mS)
Suppression sensitivity:	-31 dBmO +/- 0.3 dB at 1000 Hz
Break-in sensitivity:	-31 dBmO +/- 2 dB at 1000 Hz

Echo suppressors at present represent the most widely used means of reducing echo levels, due mainly to their economic advantage over the much more complex and expensive canceller. At the time when suppressors were originally developed, cancellers were not considered because of the

technology of the time.

1.3.2 Echo Cancellation

With the problems experienced by echo suppressors on long delay circuits, and with advances in technology appropriate to real-time signal processing, echo cancellation has received much attention recently. The basic principle is to model the echo path in the form of a filter, to generate a replica of the expected echo, which is then used to cancel the echo that is received. A diagram illustrating this principle is shown in Fig. 1.8.

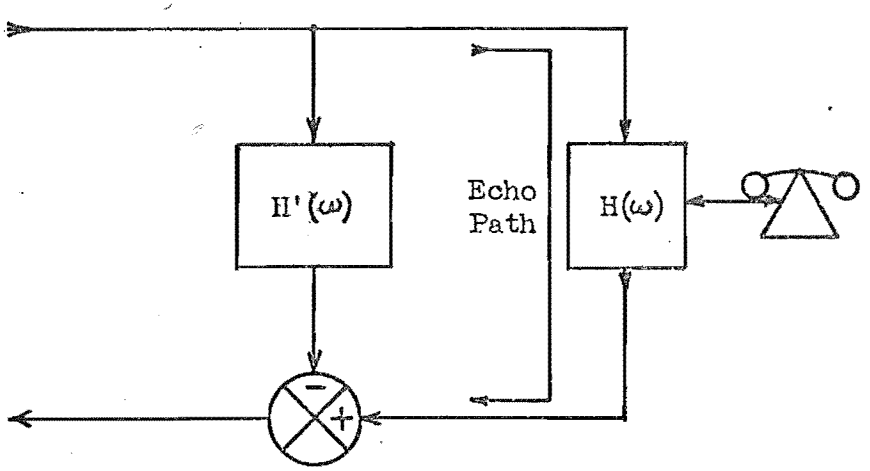


Fig. 1.8 Echo Canceller Operation

The diagram in Fig. 1.8 is, of course, a gross over-simplification of the process involved but illustrates the principle. The automatic modelling of the transfer function $H(\omega)$ by $H'(\omega)$ is a complex and expensive process, and the means of obtaining the echo path characteristics are varied. Once the circuit characteristics are established, however, the principles behind the filter

realisation are similar in all cancellers.

The realisation of the filter is based on the convolution theorem. The proof of this theorem is given in Appendix II. The theorem states that the product of two functions in the frequency domain, has an equivalent operation in the time domain described by the convolution integral. In the canceller the product of the frequency domain representations of the speech and filter characteristics $S(\omega)$ and $H'(\omega)$ respectively, is replaced by the convolution of the time domain representations of the two functions.

$$E'(\omega) = S(\omega) \times H'(\omega)$$

becomes $e'(t) = s(t) * h'(t)$ --- convolution theorem

or $$e'(t) = \int_{-\infty}^{\infty} h'(\tau)s(t-\tau)d\tau$$ --- convolution integral

For signal processing this continuous case reduces to the discrete approximation, where samples of $s(t)$ and $h'(t)$ only are known, and they obey the sampling theorem. The equation for the discrete case becomes:

$$e'(kT) = \sum_{-\infty}^{\infty} h'(iT)s\{(k-i)T\}$$ for k and i integer

T is sample period

The practical realisation of this equation limits the impulse response of the echo path $h'(kT)$ to $0 \leqslant k \leqslant L$, and $e'(kT)$ is only calculated for one value of k, normally $k = 1$, as time $k = 0$ is generally considered to be a varying

time reference. It is convenient to consider k = 0 to be the time the most recent sample of the speech waveform was taken. As only in an infinite bandwidth system will h'(iT) have any value at i = 0, the summation is further restricted to $1 \leqslant i \leqslant L$.

The discrete convolution equation realised by the filter then becomes

$$e'(1T) = \sum_{i=1}^{L} h'(iT)s\{(1-i)T\}$$

This, therefore, generates the estimate of the value of the echo waveform at time 1T after the last speech sample was taken. The equation requires speech samples s(kT) for the time period $0 \leqslant k \leqslant (1-L)$ which must be held in memory, as must the L samples of h'(kT).

As was established earlier, the length of the impulse response required is 32 mS including the delay prior to the active period. With the maximum frequency less than 4 kHz, a sampling rate of 8 kHz is satisfactory and is an accepted standard in time division multiplexed systems. The sample period is, therefore, 125 μS, meaning that 256 samples are required to make up the discrete impulse response h'(kT). In the final form the discrete convolution equation becomes:

$$e'(1T) = \sum_{i=1}^{256} h'(iT)s\{(1-i)T\}$$

Another aspect of echo characteristics published by CCITT[12], which is used to advantage in the first prototype canceller, is the concentration of energy within the 8 mS of

activity. By knowing that only 8 mS or 64 samples of h'(kT) need be non zero, the length of the convolution equation can be reduced with an appropriate delay introduced. However, at this point the impulse response will be considered to be 256 samples long.

The echo canceller can be realised either digitally or with analogue circuitry. With the advances in digital signal processing technology, especially in the area of memory, the trend is towards digital implementation. Another of the variables in canceller design is the method of obtaining the impulse response samples as filter coefficients. The main thrust of research in this field has been towards a digital adaptive canceller which continually adapts its filter coefficients to minimise the echo. This enables variations in echo path characteristics to be followed, with the system converging to a satisfactory level of cancellation in the order of 1 sec. This method has its own set of problems as do other methods. Each alternative type of canceller will be dealt with individually to ascertain its relative advantages and disadvantages.

1.3.2.1 Non-Iterative Echo Canceller

One of the first canceller designs was by Akira Miura and others in 1969. This model was the simplest of all designs. Although having some basic practical problems, it is particularly attractive because of its simplicity and resultant low cost. A schematic diagram of this canceller is shown in Fig. 1.9.

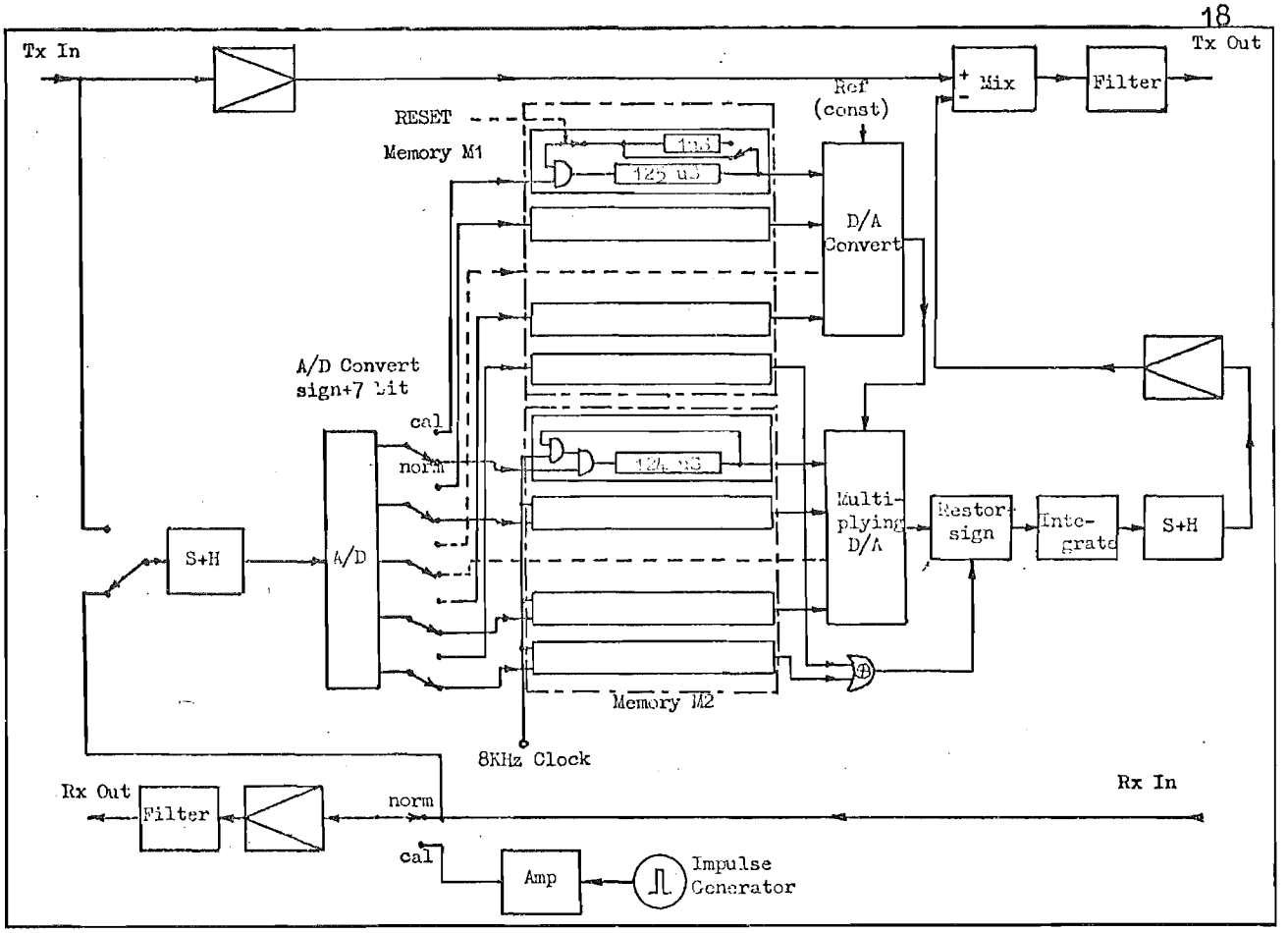


Fig. 1.9 A Blockless Echo Suppressor.
Reproduced from Ref. (63)

To measure the impulse response of the circuit an impulse is transmitted around the echo path, and the response of the echo path measured directly. The resultant filter coefficients are stored in digital delay lines. The speech samples are also stored in digital delay lines with both sets of samples being recirculated around the delay lines to permit access to them. Once entered the filter coefficients do not change, whereas for each new speech sample, the signal samples are advanced one position in the line. Consequently, the sample that has been in longest is lost. The products of the digitally represented samples

are achieved with multiplying Digital to Analogue (D/A) convertors. The output from the D/A convertor on the output of the stored coefficients provides the reference for the convertor on the speech samples. Results of tests illustrated that with 8 bit quantisation of coefficients and speech samples, a cancellation of 20 dB could be achieved. This reduction in echo level is termed Echo Return Loss Enhancement (ERLE).

The main disadvantage of such a system is that the presence of any noise or subscriber's speech at the time of impulse response measurement will cause errors in the filter coefficients. This 8 bit linear quantisation also means quantisation noise error will be only 48 dB below the maximum level expected - or approximately 28 dB below the R.M.S. value of active speech. Dalhgaard & Nielson[33] found the R.M.S. value of active speech to be 17 dB below the R.M.S. value of the maximum level accommodated, or 0 dBm0. This noise will be present even in the absence of speech. A further complication is the necessity to check for unsatisfactory cancellation due to random and sometimes continuous changes of echo path characteristics.

1.3.2.2 Analogue Adaptive Echo Cancellers

The analogue adaptive canceller requires a vast amount of analogue circuitry to achieve the processing required. The products of the convolution equation are formed by analogue multiplication with a multiplier required for each coefficient. Furthermore, another multiplier is required to generate each coefficient which

is obtained by correlating the cancelled echo with the speech samples. A simple explanatory diagram reproduced from Gould & Helder's paper[45] is shown in Fig. 1.10. The complexity of the operation, using analogue multipliers, becomes clear on studying this diagram.

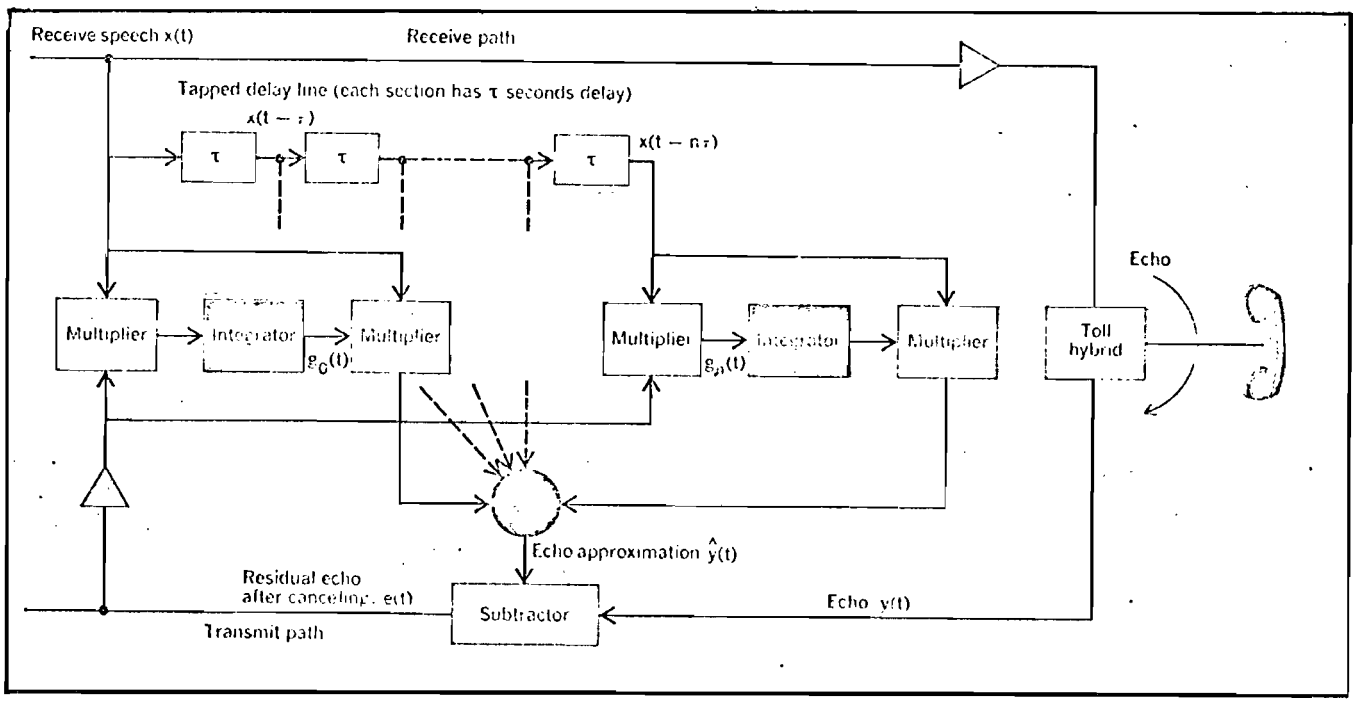


Fig. 1.10 Analogue Adaptive Echo Canceller.
Reproduced from Ref. (45)

Operation of the circuit is as follows: Received speech samples x(t) are passed down a tapped analogue delay line, each tap output being multiplied by a filter coefficient before summing with all other products to form the echo estimate. The filter coefficients are generated by correlating the output of each tap with the cancelled echo. If there is no correlation the coefficient remains unchanged, but if there is some correlation then the value of the coefficient is 'steered' in the direction to decrease

this correlation. There are various algorithms for such a corrective process. This then represents the principle not only of analogue but also of digital adaptive cancellers. The main disadvantage with analogue realisations is the necessity to have multipliers for each coefficient resulting in duplicated circuitry. For this reason and others, analogue cancellers have found little favour with researchers in this field.

Experiments by Brueggemann and others[5,6] working at the Australian Post Office Laboratories have also been based on the analogue adaptive canceller. A variation in the form of an initial transmission of a pseudo random noise sequence for the filter to converge on is used, resulting in an initial convergence in 160 mS. Cancellation of around 20 dB was achieved.

1.3.2.3 Digital Adaptive Echo Cancellers

The most comprehensive research, development and operational testing of echo cancellers has been undertaken by COMSAT under the sponsorship of INTELSAT. This commenced with an initial paper by Kato and others[91] describing a prototype canceller. This first prototype incorporated an initial calibration where a single pulse was transmitted and the response sampled as in the case of the non-adaptive canceller described earlier. From that time on, the canceller was allowed to adapt to circuit changes. Shift registers were used for the storage of speech samples and filter coefficients. Initial testing indicated an echo return loss enhancement of around 20 dB which they

considered inadequate. The convergence time of the adaptive structure was around 1 sec, and this was unsatisfactory for following anything but slow rates of phase roll.

Improvements on this basic canceller design in terms of the convergence algorithm were reported by Campanella and others[30]. The initial calibration pulse was abandoned and it became a completely adaptive canceller. The convergence time reduced to about 500 mS, and an echo return loss enhancement of 21 dB was achieved when converging on noise. For convergence on speech, a reduction of about 3 dB in ERLE was suffered. More detailed tests were carried out on the effects of phase roll, and it was found that the reduction in ERLE was between 2.4 dB/rad/sec and 6 dB/rad/sec as the noise being used as a test signal varied from -10 dBm0 to -30 dBm0 respectively. A block diagram of this canceller is shown in Fig. 1.11.

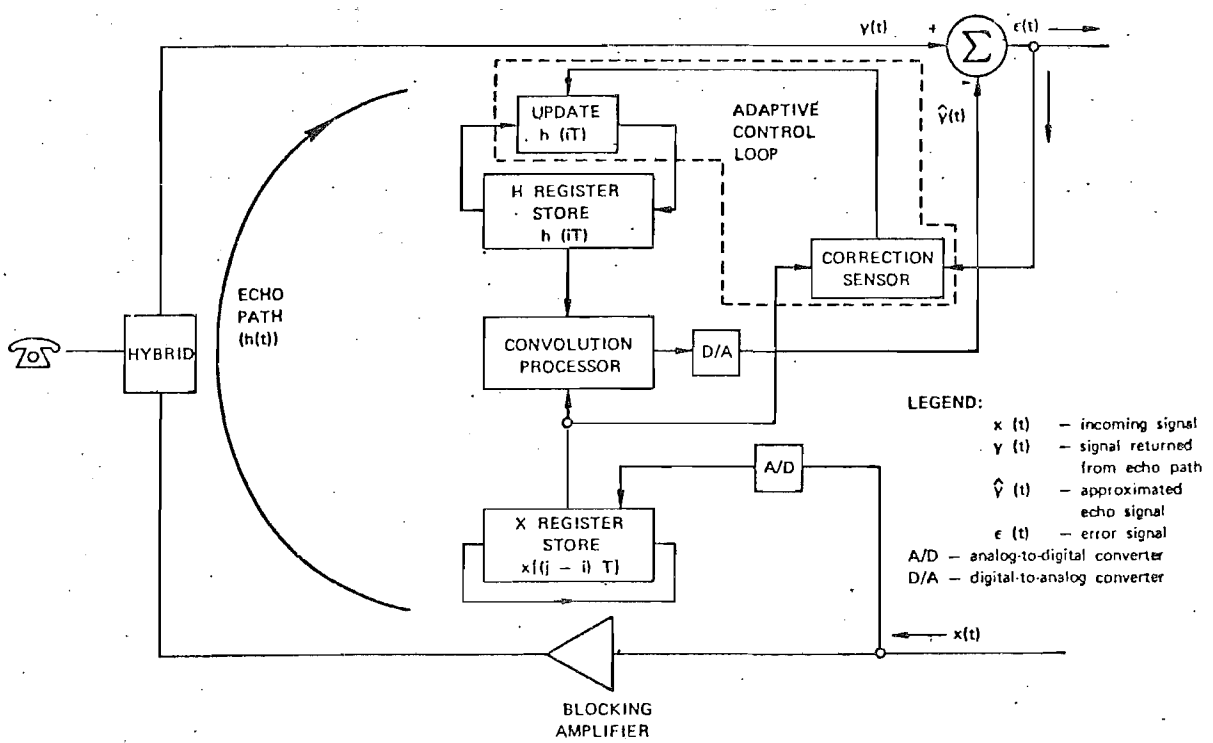


Fig. 1.11 Block Diagram of Digital Adaptive Echo Canceller. Reproduced from Ref. (30)

The first results of field trials on this canceller were published by CCITT[24] on initial tests between the United States and the United Kingdom. The echo canceller performance was understandably compared with that of the echo suppressor. In about 80% of the cases, cancellers showed an improvement over the suppressor and in the other 20% no significant difference was noted.

More detailed technical results were reported by Suyderhoud and others[81] in 1975, following world wide field trials. Convergence time of 3 words of a conversation and echo return loss enhancement figures in the order of 25 dB were achieved. No cases of phase roll were noted and therefore no conclusions were drawn on the ability of the cancellers to follow it. It was accepted that the canceller would not work satisfactorily for phase roll rates greater than 0.5 Hz. The subjective assessments showed that cancellers significantly improve the quality of the call where echo is the primary problem. An important conclusion at this stage made by the authors was that the designs exceeded the limits of economic viability. Results of these same tests were also reported by CCITT[26].

Another major contribution in this field has been made by workers at Bell Labs. One of the first to work on adaptive cancellers was Sondhi[80]. The first canceller designed by Sondhi also relied on the initial transmission of an impulse, followed by an adaption process to follow time variances.

The effect of noise on the operation of adaptive cancellers was studied by Rosenberger and Thomas[76]. The aim of this was to determine the effect of double talk on the performance of the adaptive section. It should be realised that these tests were limited to circuits which were time invariant. It was found that during convergence on speech it converged on a frequency selective basis, the fit being best in that portion of the spectrum where most energy was concentrated. Conversely, double talk caused a divergence also on a frequency selective basis. For this reason it is normal not to permit the filter coefficients to adjust during double talk. Any time variance must therefore be adjusted to following the period of double talk, therefore limiting its ability to handle phase roll.

Gitlin and Weinstien[43] working at Bell Labs. also studied the effect of interference on the tracking ability of digital adaptive cancellers. Although restrictions needed to be placed on the step size of any adjustment, they showed that convergence was possible in the presence of double talk. This was desirable and in fact necessary in the case of long periods of double talk as encountered in the case of data transmission.

Gitlin and Thompson[42] proposed a phase adaptive structure at a time when this author had developed just such an approach. The intentions are witnessed by an article by Webb and Kelly[87] on the use of a tapped delay line to generate a quadrature component of voice. By combining the true and quadrature component in the correct

proportions any phase shift can be generated. The phase tracking can therefore be handled as a separate problem without varying the filter coefficients. Further details on this approach are given in chapters 5 and 6 as a contribution by this author. Gitlin and Thompson[42], however, persist with the normal adaptive structure as well as the phase adaptive structure.

A 12 channel digital adaptive canceller was designed at Bell Labs. by Duttweiller[39]. The time sharing or multiplexing of components was shown to make the otherwise conventional adaptive canceller more economically attractive.

Working at the Research Department, Telecom Australia, Demytko and English[35] have studied the effect of time variance and, specifically, phase roll on the performance of echo cancellers. They show that a high speed adaptive canceller can satisfactorily handle phase roll up to 2 Hz. High speed adaptive cancellers are, however, susceptible to noise or near end speech and are not widely used. This of course is an example of the common compromise in control systems of a fast response being traded for noise immunity. The attention paid to phase roll in Australia is due to the relatively high probability of encountering this effect on the Australian telephone network.

The coding of speech and impulse response samples in a pseudo logarithmic format was proposed by Horna[54].

This is similar to the true logarithmic coding proposed in this thesis, and results in simplified generation of products in the convolution process. The use of the A-law companding code, as used by Horna, introduces errors when it is assumed in the processing that these are in fact true logarithms. It will be shown in chapter 4 that true logarithmic coding can be achieved despite the problem of taking logarithms of numbers near zero.

The main distinguishing feature of the cancellers described in this thesis is their non-adaptive nature and resulting simplicity and cost advantage, without any compromise on performance.

1.3.3 Area of Research

The major factor inhibiting the widescale introduction of echo cancellers is the high per channel cost compared with suppressors. The main reason for the continued interest in the adaptive structure appears to be its ability to follow time variances. As they are in fact unable to follow satisfactorily phase roll of greater than about 1 Hz it seems a new approach is justified.

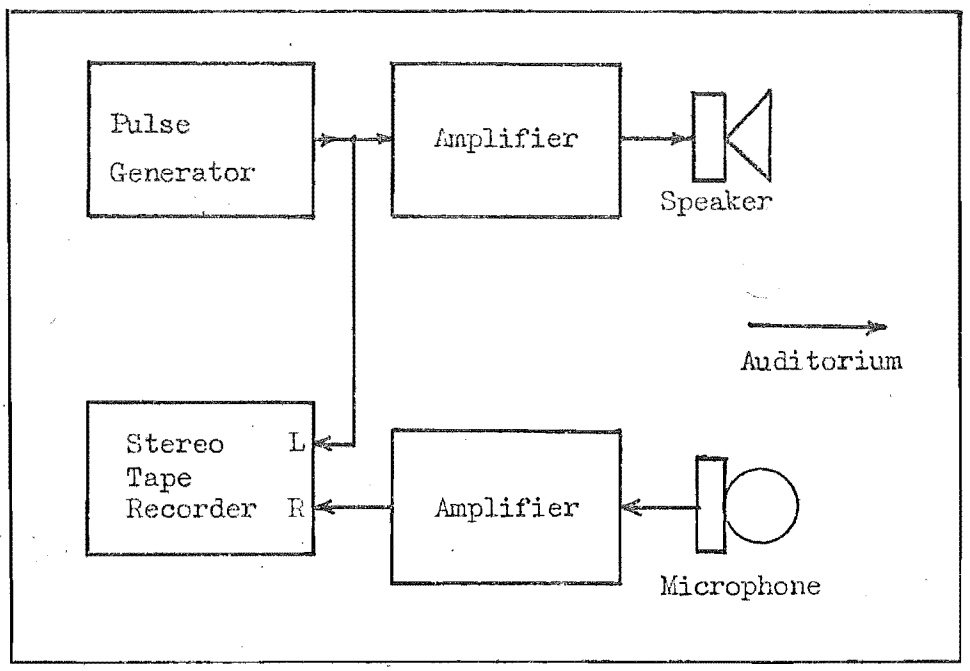
It was therefore decided to adopt a direct measurement approach in finding the filter coefficients. As phase roll can be ignored on New Zealand circuits, an economical unit should be able to be designed. To give the canceller wider application, the problem of phase roll is treated separately. Any intermittent time variance is accommodated by a complete re-calibration.

For a canceller to be a viable alternative to the suppressor it should have advantages proportionate to its extra cost. Existing cancellers do not meet this requirement.

1.4 ECHO CONTROL IN AN AUDITORIUM

Although not directly related to communications circuits, the processing of the sound signal using similar techniques to those used in echo cancellers, could artificially enhance the acoustic properties of an auditorium. There are two aspects which the author considers as possible applications for these techniques. The first is the more directly related one of reducing echoes to prevent feedback causing instability. The second is to model the characteristics of an ideal auditorium as a transversal filter. To establish the feasibility of such a proposal, some measurements were made of the impulse response of the Ngaio Marsh theatre at the University of Canterbury. A photograph of the response of the auditorium at the microphone, to the transmission of an impulse is shown in Fig. 1.12, along with the test setup used for this measurement.

As the length of the response is about 500 mS for 90% of the energy, about 4000 samples of the impulse response would need to be used in the transversal filter to achieve a 10 dB reduction in the feedback at the microphone in a 0-3000 Hz public address system. This corresponds to a 8000 Hz sampling rate, and therefore



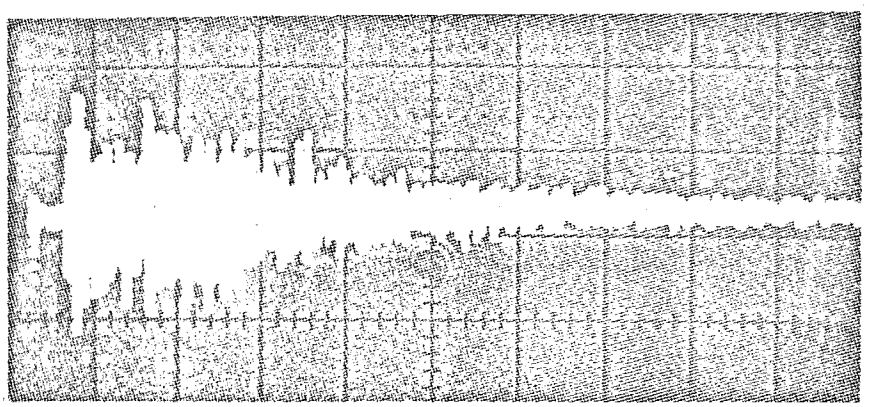


Fig. 1.12 Impulse Response and Test Setup for Ngaio Marsh Theatre.

4000 sample pairs must be multipled every 125 μS using the same principles as discussed for echo cancellation in the previous section. As this impulse response of the auditorium was measured for an empty auditorium, it is expected that it would be shorter for a full auditorium. The worst case, however, must be catered for.

The other aspect of echo control has potentially more to offer and in itself would also overcome the problem of instability due to feedback. By modelling the transfer function of an ideal auditorium as a transversal filter, the sound can be transmitted as though it had already been subjected to it. If it is transmitted into a dead auditorium, with no echoes, then it should sound as it would in that ideal auditorium. As the cost of physically constructing such auditoriums increases, the attractiveness of such a proposal becomes obvious. The application of this to outside theatres would also enhance the sound in an otherwise difficult environment.

If a 0-15 kHz bandwidth is required, a 30 kHz minimum sampling rate would be needed. This is based on a high quality audio system for such applications as orchestral concerts. For an impulse response length of 500 mS, 15,000 samples of it are required. This also means that 15,000 sample pair products must be calculated every 33 μS. Although this seems impractical, with the speed of modern technology this may not be the case in the future. The advantage of this application over that of cancelling the echo is that the impulse response of

the ideal transversal filter remains unchanged, which simplifies the circuitry. It is also possible that parallel processing would make this technically feasible now.

No further work has been carried out by the author on this proposal to date.

CHAPTER TWO

FIRST PROTOTYPE ECHO CANCELLER

2.1 INTRODUCTION

The main feature of this canceller was in its use of Random Access Memories (RAMs) for storage of impulse response and signal samples. This enables the samples to be accessed simply and efficiently reducing the speed required for processing. An experimental technique of scaling the impulse response and signal samples provided for a reduction to 5 bit digital representation enabling simple digital multiplication. Multiplication was achieved by using a Programmable Read Only Memory (PROM) as a multiplication look-up table with the two 4 bit magnitudes providing the address and the output being the product of the two.

2.2 NEW TECHNIQUES

To enable the representation of signal and impulse response samples by 5 bit digital representation it was necessary to provide some form of gain control around the filter. This is best understood from an explanation of the scaling required for the impulse response samples.

2.2.1 Impulse Response Scaling

As the echo level can vary up to 20 dB due to variations in the mismatch at the hybrid, then obviously the peak value of the response will vary by a similar amount. If, for example, 8 bit quantisation is used, the gain prior to A/D conversion is adjusted so as the maximum peak expected will represent a full scale input to the converter and will be quantised to +/- 128 levels. This limits the possible echo reduction to 20 log 128 = 42 dB. However, an impulse response having a peak of only 1/10 the maximum peak expected will be quantised to only +/- 12 levels. The result is a possible echo reduction of only 20 log 12 = 22 dB. By adjusting the gain around the filter the peak of each impulse response represents full scale input to the A/D converter and hence equal quantisation and similar echo reduction is achieved.

In this echo canceller only 5 bit representation was used with the gain being adjusted so that the impulse response was quantised to +/- 15 levels. This was achieved by transmitting two pulses for calibration purposes. The first was used to determine the unscaled peak amplitude which was stored and used to control the gain so that the peak amplitude of the response to the second pulse would be quantised to the full +/- 15 levels. This gain control prior to sampling took the form of a divider whose gain was inversely proportional to the control voltage which was derived from the peak value of the unscaled impulse response. The control

voltage also determined the gain of a multiplying D/A converter which compensated for this gain adjustment after the filtering.

2.2.2 Signal Sample Scaling

A similar arrangement provided for the scaling of the signal samples, although this was expected to be less satisfactory. The scaling factor was derived from a peak detector charging circuit and the gain adjusted by using this peak detector output to control the divider circuit. The gain around the filter was not permitted to vary by more than ½ the least significant bit over any 32 mS period. This ensured that signal samples quantised subject to this gain control were processed with the correct gain compensation at the output for the duration of their 32 mS storage period in the canceller. This requirement was not difficult to obtain for the decaying control voltage but difficulty arose with the occurrence of a new signal peak. The peak detector output at any time represented the current full scale input of the A/D converter. For a new and larger peak to be quantised the gain was immediately altered so that the new peak was represented by the full scale input to the converter. This meant that all samples stored in the previous 32 mS were processed with the wrong compensatory scaling at the output. This would cause a burst of echo of 32 mS duration. The severity of this would have needed to be determined subjectively. Scaling enabled the 5 bit representation of signal samples also.

2.2.3 Storage of Impulse Response and Signal Samples

Perhaps the greatest advantage of this echo canceller was in its incorporation of high density solid state memory. In using RAMs for storing the signal and impulse response samples, a more convenient method of accessing samples was available. This compares favourably with existing methods of rotating samples around a shift register to enable access to them as they appear at the output. With RAMs it was merely a case of counting through the consecutive memory addresses.

This permitted another major improvement over existing methods. Although a total period of 32 mS was considered in the convolution it was known that only 8 mS of that period had non zero impulse response samples. This meant that only 64 samples of impulse response need be stored and only 64 of the 256 signal samples need be accessed for multiplication each sample period. By determining the delay to the active period of the impulse response by detecting the position of the unscaled impulse response peak, the delay prior to the beginning of the active period was calculated. The peak must occur within the first 1 mS of the active period (see Fig. 2.1) and, therefore, the impulse response samples are stored from a time 1 mS prior to the time of the peak to 7 mS after the peak. This initial delay has previously been accommodated by incorporating a separate delay for signal samples or by carrying out the convolution over the full 32 mS (256

samples) period. By using RAMs all previous 32 mS of signal samples are stored but only the 64 corresponding to the active period need be read each sample period. This negated the requirement for separate signal delay or the extra speed required to convolve 256 sample pairs. A pictorial representation of the storage of samples in RAM can be seen in Fig. 2.2.

2.2.4 Accessing and Multiplying Sample Pairs

The 64 impulse response samples were stored in RAM in binary address positions 000000 to 111111, with the first sample of the active period (- 1 mS on delay to peak) appearing in address 000000. The position of these impulse response samples in memory remained unchanged. To access these samples for multiplication it was necessary to count through the memory address 000000 to 111111.

The storage of signal samples is slightly more complex. The first signal sample could be stored anywhere but each subsequent sample was stored at the binary address preceding that of the previous sample. A new sample was stored every 125 uS corresponding to an 8 KHz sampling rate. As signal samples were stored for 32 mS, 256 bytes of storage were required representing an 8 bit (0 to 255) address. If the previous sample was stored at address 00000000 the next address for storage would be 11111111. The write address could then be provided by a decrementing 8 bit binary counter clocked at 8 KHz.

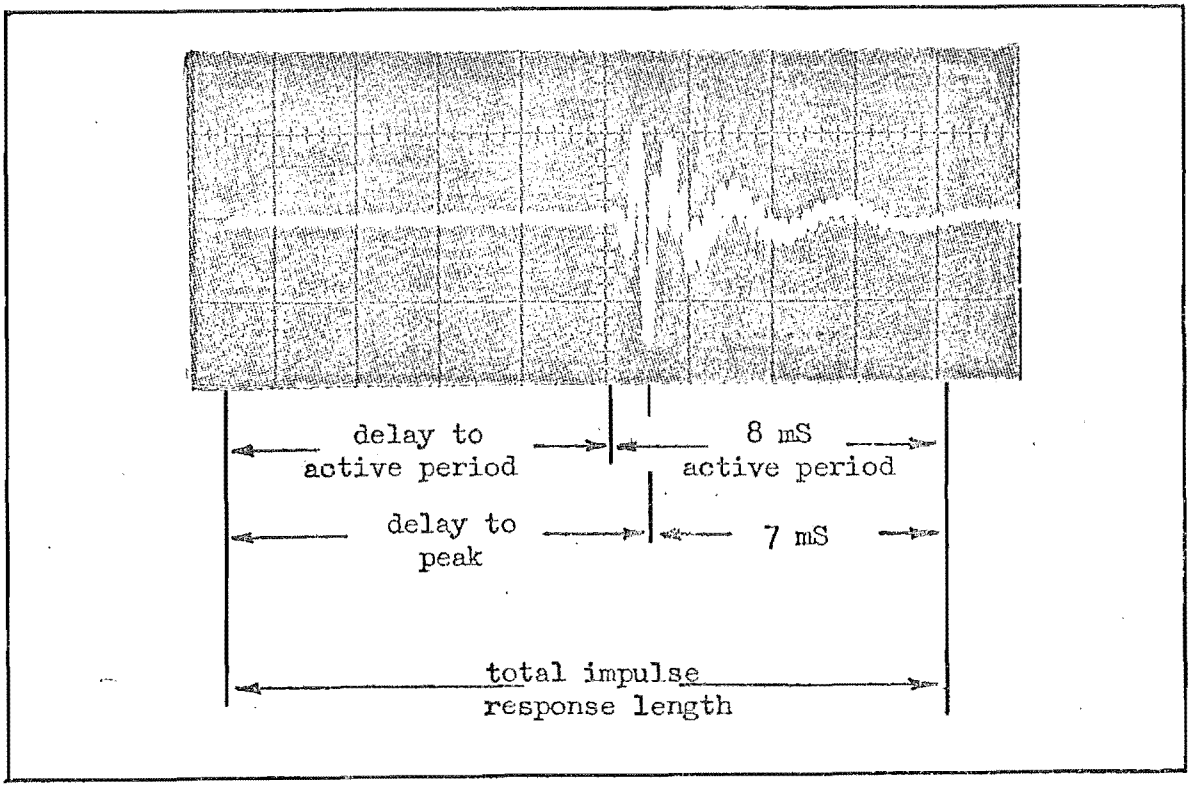


Fig. 2.1 Typical Impulse Response

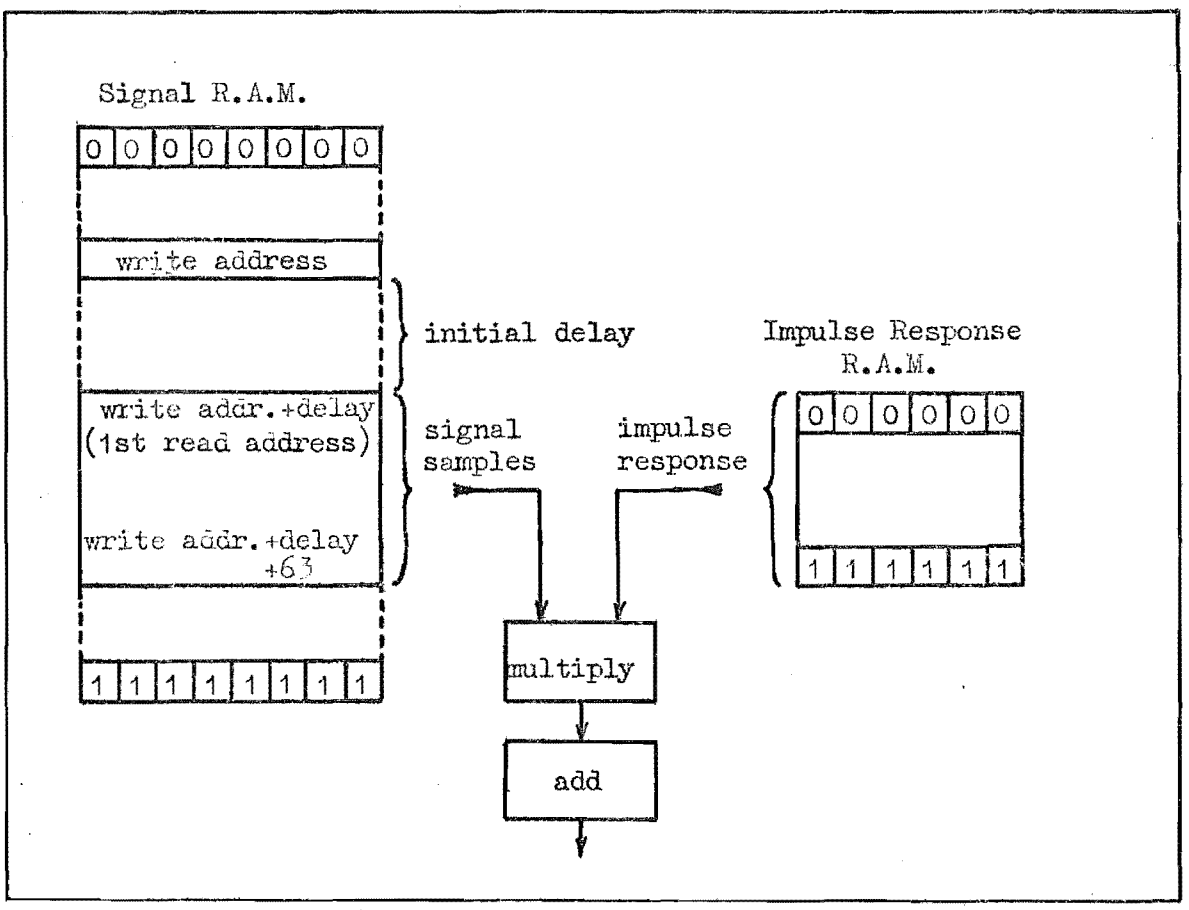


Fig. 2.2 Storage of Signal and Impulse Response Samples

The address from which the 64 samples must be 'read' for multiplication were determined from the delay prior to the active period of the impulse response. If the delay to the peak was 1 mS then the delay to the first impulse response sample would be zero and the address of the first signal sample to be read would be the current write address. The next 63 samples were those in the next highest 63 addresses. These are the last 64 signal samples stored. If the delay to the impulse response peak was 5 mS, the delay to the active period is 4 mS, and the first read address would be the current write address plus 32 representing a delay of 4 mS or 32 samples. A pictorial representation of this is found in Fig. 2.2.

With the read addresses for the impulse response and signal samples being incremented concurrently the sample pairs were used as an address for a PROM which had as its output the product of the 4 bit magnitudes. As the samples are stored in a sign and magnitude format the product of magnitudes is provided by the PROM. The 5 th bits (sign bits) are checked for parity, a lack of parity indicating a negative product, which is 2's complemented for use by the digital accumulator. A diagramatic representation of this process is shown in Fig. 2.3. A more rigorous explanation of the calculation of the first read address follows.

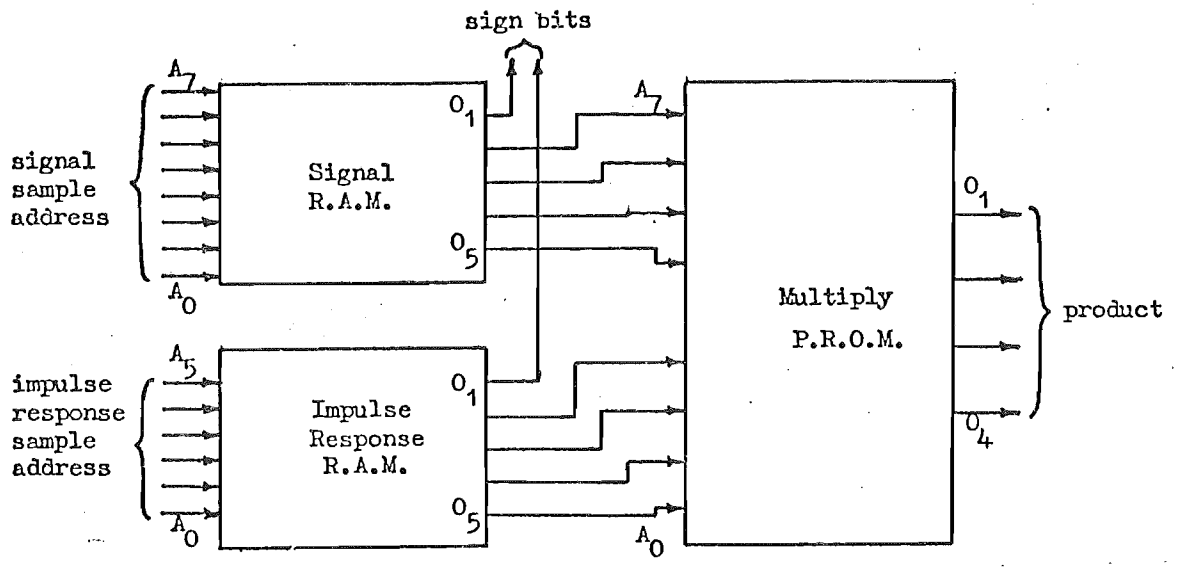


Fig. 2.3 Generation of Products

The first read address is derived from the discrete convolution equation:

$$y(kT) = \sum_{i=0}^{N-1} h(iT) \cdot x((k-i)T)$$

As it takes one sample period to calculate the expected value of the echo at a given time, it is convenient to calculate it for a time of one sample period (1T) after the latest signal sample is taken.

Now the total impulse response and set of signal samples cover 256 sample periods so:

$$N = 256$$

k is required to be 1 as we are to calculate the value for 1 sample period T after the time of sampling defined to be t = 0 for convenience.

If h(t) is the impulse response and is zero for all 't' less than aT and for all 't' greater than bT then we only need consider h(t) over the period $aT \leqslant iT \leqslant bT$. As we have determined (b - a)T = 8 mS then b - a = 63 and b = a + 63. The summation therefore becomes:

$$y(T) = \sum_{i=a}^{63+a} h(iT) \cdot x(1 - i)T$$

where 'a' is the delay in sample periods to the first impulse response sample. The first read address for speech samples is (a + 1) greater than the current write address as $\dot{x}\{(1 - i)\}T$ goes from $\dot{x}\{(1 - a)T\}$ through to $\dot{x}\{(1 - 63 - a)T\}$.

2.3 CONVENTIONAL CIRCUITRY

Apart from the specifically mentioned features of the circuit, it was conventional as far as echo cancellers are concerned. A block diagram is shown in Fig. 2.4 of the complete canceller.

The incoming speech which generated the echo was sampled and held and converted in the A/D converter. The complementary offset binary output was converted to sign and magnitude format prior to storage in memory.

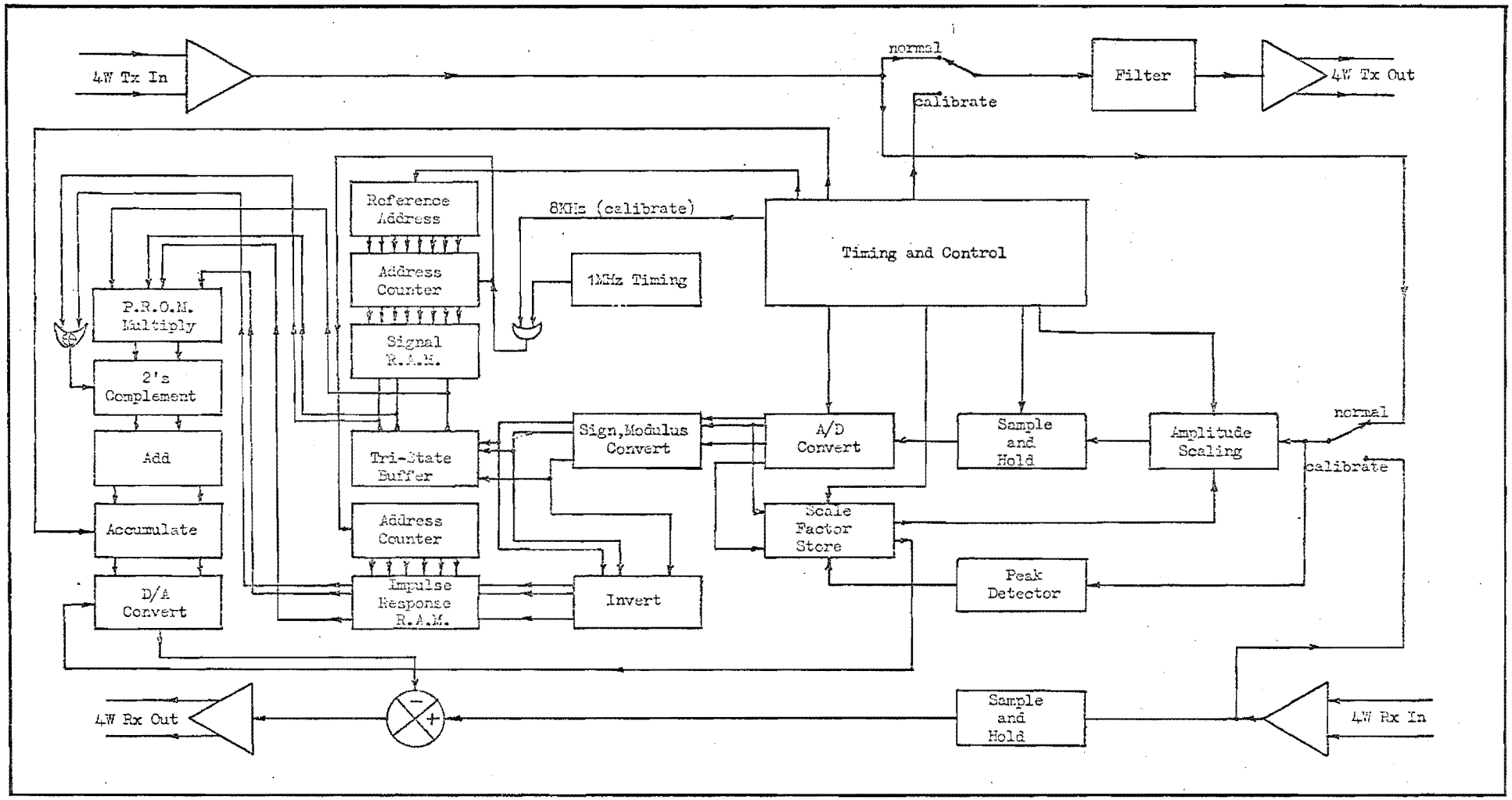


Fig. 2.4 Block Diagram of New Echo Canceller

Following the multiplication of the sample pairs the summation required to complete the discrete convolution was achieved with adders whose output formed the second adder input by means of a latch which held the interim summation. At the end of each sample period the output from the latch was converted to analogue and scaled in amplitude according to pre-filter scaling by utilising the multiplying capability of two D/A converters. This gave an estimate of the amplitude of the echo at that time, which was subtracted from the natural echo in a differential amplifier.

A complication which arose which appeared to have been neglected previously is that this estimate is only defined at one point in time. This was overcome by 'holding' this value until the next value was calculated one sample period later. The act of holding this value modified it in a way that meant it no longer was a correct estimate of the natural echo unless the natural echo was subjected to the same modification. The effect of the holding circuit is explained in detail in Appendix III, but essentially acts as a sin x/x low pass filter, with the first zero of response being at the sampling frequency. Unless both the estimate and the natural echo are subject to its affect accurate cancellation cannot occur. This was overcome by sampling and holding the natural echo also prior to cancellation.

The impulse response in this experimental design was obtained by measuring the echo path response to a 5 uS rectangular pulse. As the bandwidth of the pulse is much wider than that of the system it can be considered to approximate a true delta function and have the characteristics of white noise.

2.4 PREDICTED PERFORMANCE

Calculations were initially based on a 5 bit representation of signal and impulse response samples. This was followed by calculations of the improvements expected by scaling the sample amplitudes. It resulted in a 20 - 24 dB reduction in echo level being expected.

2.4.1 Impulse Response Quantisation

As the A/D converter had a specific zero level to eliminate quantisation noise for no signal operation, there are + 16 and - 15 levels of quantisation and the magnitude must effectively be represented by 15 levels. The smallest magnitude recognised would, therefore, be 1/30 (½ LSB) of the maximum expected peak value of the impulse response. This meant any echo less than 1/30 of the maximum expected would not be 'seen' and hence this limited echo cancellation to 20 log (1/30) = - 29.5 dB on the maximum expected. The ½ LSB also represented the accuracy to which a sample was quantised giving the same limit to cancellation. Quantisation noise must also be considered and the mean value of this would be 20 log (¼ x 1/15), or - 35.5 dB below the maximum

expected response peak.

This, therefore, limited the performance of the canceller to providing a minimum echo level of - 29.5 dB below the maximum expected echo level. As the mean echo level is reported by CCITT[12] to be around 15 dB below the worst expected this indicates a mean echo reduction of only 14 dB.

2.4.2 Signal Sample Quantisation

With the peak magnitude of the signal value adjusted for full scale input to the A/D converter (+/- 15 levels) then any signal below ½ LSB would not be 'seen'. Any signal values below - 29.5 dB would, therefore, not contribute and the accuracy of quantisation would also limit cancellation to - 29.5 dB relative to the echo generated by the peak signal. The ineffectiveness of this is realised from the study by Dahlgaard[33]. Dahlgaard shows the mean energy level over the active period of conversation to be - 17 dB relative to the maximum possible R.M.S. level. The mean reduction in echo level, therefore, could only be 12.5 dB with 5 bit quantisation.

Quantisation noise must again be considered and this would again be 35.5 dB below the maximum level or 18.5 dB below the mean signal level. Having a zero magnitude level out of the A/D converter ensured that no quantisation noise would be generated during no signal operation. Quantisation noise would only be generated as an echo while the person was speaking thus avoiding degradation of service.

2.4.3 Improvements Due To Scaling the Impulse Response

The basis of the scaling procedure was to adjust the gain before and after the discrete convolution process to utilise all 31 levels of quantisation. With the peak value of the impulse response known to be +/- X volts and the range of the A/D converter +/- 2.5v the gain before quantisation was adjusted to set the peak value at +/- 2.5v. If X is less than 2.5v the gain was increased prior to quantisation and decreased after convolution.

The range over which this scaling procedure could operate was determined by the accuracy of the gain adjustment stages. The gain prior to quantisation was inversely proportional to the peak value of the response and an analogue divider was used. The gain after convolution was proportional to the peak value and a multiplying D/A converter was used. The divider circuit determined the range of operation as it was less accurate than the multiplier. It was determined experimentally that the divider provided gain control over a 15 dB dynamic range with an error of less than ½ LSB. The output voltage from the divider is defined as:

$$V_o = (10V_i/V_c)$$

where V_o is the output voltage

V_i is the input voltage

and V_c is the control voltage

By peak detecting V_i and using this as the control voltage V_c, V_o was plotted against V_i to determine its useful range. This is illustrated with the results in Fig. 2.5. The output

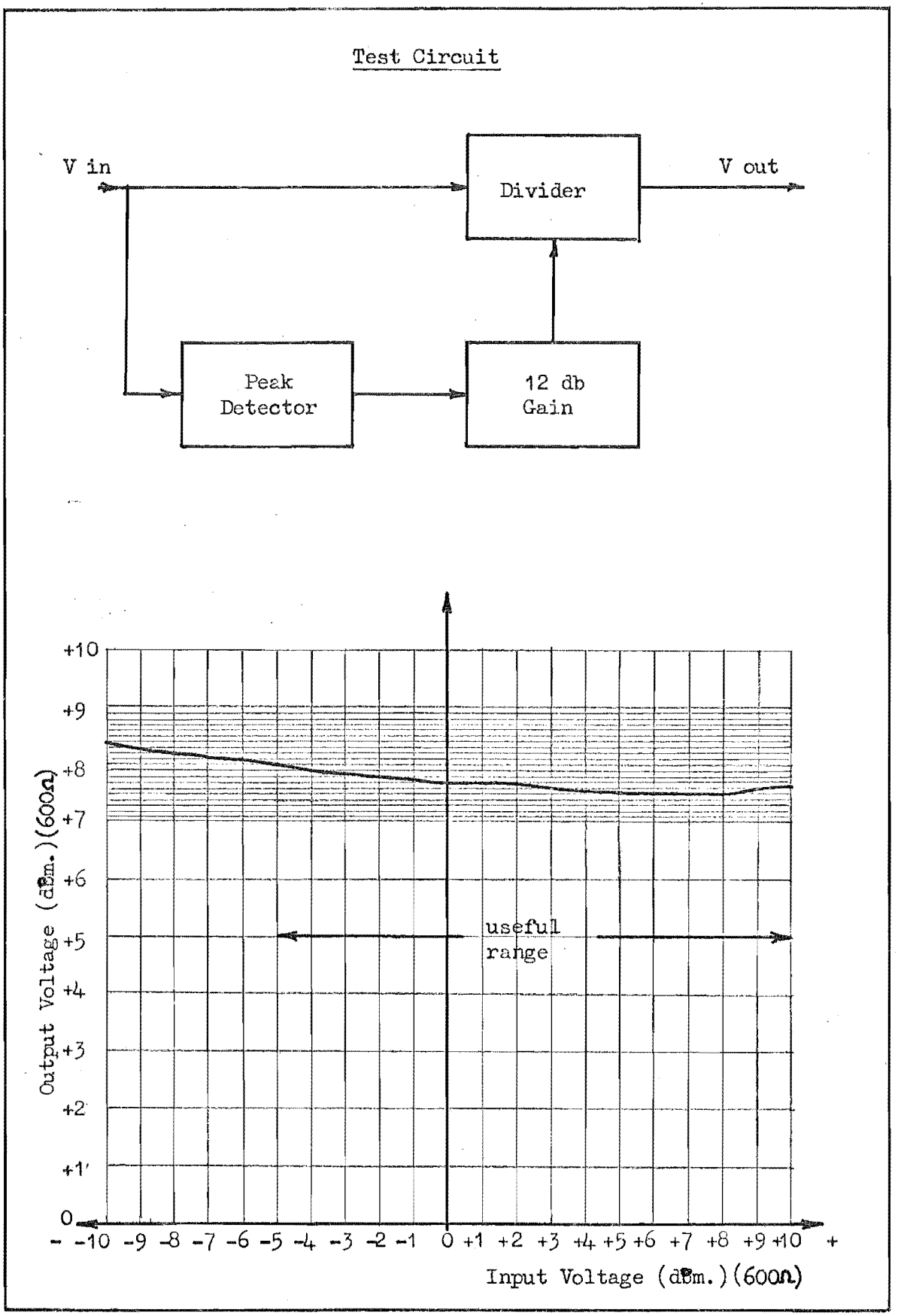


Fig. 2.5 Divider Gain Control Characteristics

voltage for the above test is ideally constant as V_c is proportional to V_i.

To achieve impulse response scaling an initial pulse was transmitted with V_c set to 10v, with the delay to the peak and the amplitude of it stored digitally. A second pulse was transmitted 60 mS later with the control voltage derived from the output of a D/A converter whose input was the peak value of the initial unscaled impulse response. Fig. 2.6 shows a diagram of the impulse response scaling procedure.

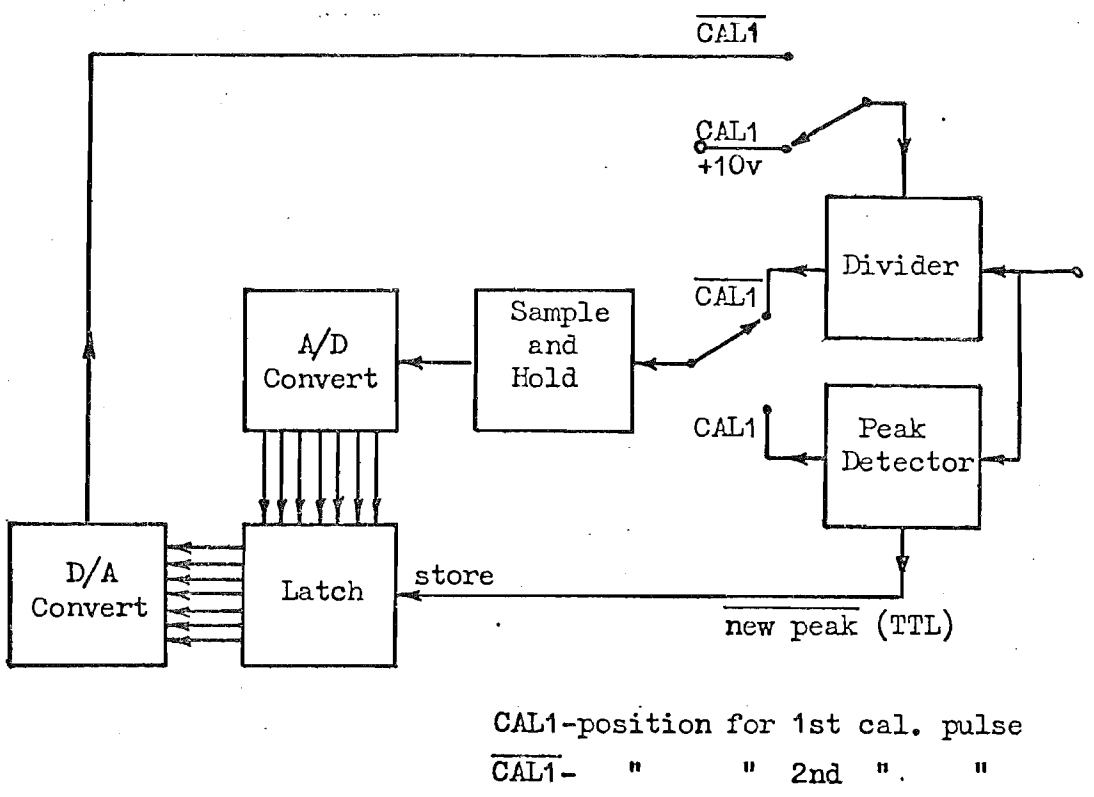


Fig. 2.6 Impulse Response Scaling Circuit

By scaling the impulse response a gain of 15 dB was achieved over the previous limitation due to quantisation to +/- 15 levels. The limitation then became -44.5 dB below the maximum expected. This then allowed up to 29.5 dB reduction below the mean echo level instead of the peak expected level.

2.4.4 Improvements Due To Scaling Signal Level

The scaling of the signal level was a less definitive process. The ideal situation was to adjust the gain of the canceller so that the peak signal sample present in storage at any one time was represented by the full scale output of the A/D converter. This was not possible as a prediction of future signal values is impossible and the gain adjustment must be changed gradually.

However, it was felt some scaling could improve the performance. The divider again provided the pre-convolution scaling with the control voltage being the output of a peak detector. This control voltage also provided the compensatory gain control using a second multiplying D/A converter after convolution. As already explained the output of the peak detector (V_c) represented the current full scale range of the A/D converter. After a peak occurred the control voltage V_c decayed at less than ½ LSB per 32 mS to avoid samples already stored, being processed according to the wrong scale factor. The gain at the input gradually increased as V_c decayed until a peak value larger than the present V_c occurred. At this point V_c immediately changed to allow this new peak to represent the full

scale value of the A/D converter. This sudden change in gain would have caused a 32 mS burst of echo. The seriousness of its effect would have needed to be determined subjectively. This was due to the previous 32 mS of speech samples being scaled and stored using a different scale factor. A block diagram of this scaling arrangement is shown in Fig. 2.7. The range of V_c was limited to a 15 dB range below the maximum value of 10v.

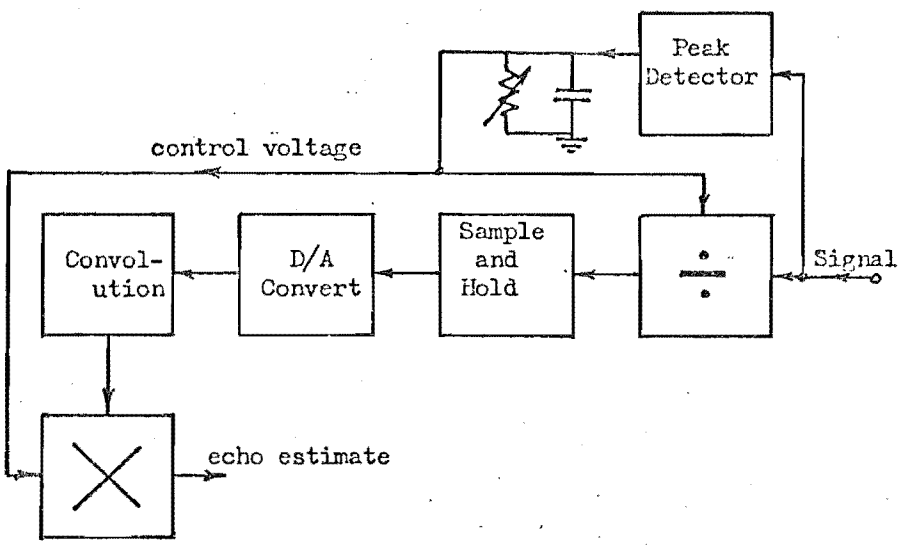


Fig. 2.7 Signal Sample Scaling Circuit

Depending on how closely V_c followed the signal peaks up to an extra 15 dB of cancellation could be expected on top of the previously calculated mean of 12 dB. A practical limit would be an improvement of about 9 dB giving an expected mean echo reduction of around 21 dB. Final figures should be determined experimentally but the above figures seem reasonable.

2.5 TEST RESULTS

Although many of the shortcomings were apparent prior to testing the device some tests on Christchurch - Auckland toll circuits were conducted. The results of these tests indicated that the canceller worked satisfactorily within the limitations of the design. Tests were carried out using tones only with no subjective assessments being made. No dynamic checks were, therefore, made of the operation of the speech sample scaling circuitry. However, by changing the gain of the echo path over a 15 dB range, the constant echo return loss enhancement indicated that the impulse response scaling circuitry operated satisfactorily within the limits of the design.

A plot showing the degree of echo reduction achieved is shown in Fig. 2.8. This does not represent mean echo return loss enhancement as the tone testing was done at a constant level and in no way represented speech.

The reason more exhaustive tests were not performed, was the now obvious shortcomings in some aspects of the design. The scaling of speech samples especially was considered unsatisfactory and clumsy. Although the scaling of the impulse response proved satisfactory, the associated process of using single pulse testing had limitations in the presence of noise. However, some form of scaling - even on a 6 dB per step (1 bit per step) basis may in future be considered. The original attraction in simplifying the multiplication process has since been

overcome by using logarithmic coding, and even modern technology in the form of digital multipliers simplifies the problem.

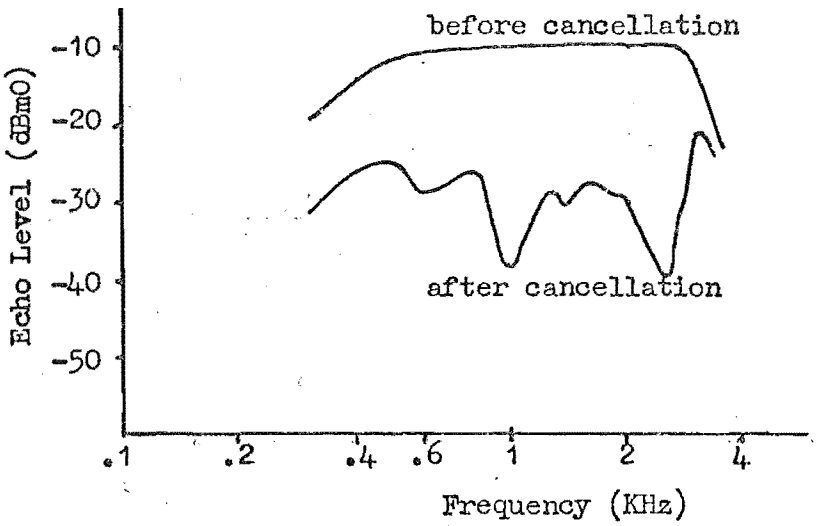


Fig. 2.8 Echo Return Loss Enhancement Results

The convenience of using modern solid state memory although expected, was at that stage significant. The advantages over the use of shift registers proposed by other researchers at that stage was obvious as there was no need to continually rotate the samples around the delay lines to gain access to them. The policy of using only the

active period of the impulse response - although successful - caused complexity which was only marginally justifiable. At the time the speed of accessing memory made the reduced length convolution attractive, but now that access time for memory is shorter the full length of the impulse response can be accommodated.

An interesting effect was noticed when the d.c. offset on the A/D converter was not adjusted correctly. When only 64 samples of the impulse response were used, with the remainder assumed to be zero, the offset effectively raises the active period onto a pedestal. This appears as a rectangular function of length 8 mS in the time domain being added to the impulse response. When the fourier transform of this function is added to the spectrum of the impulse response, the sin x/x amplitude spectrum of the pedestal with zero's at multiples of 125 Hz is clearly imposed on the spectrum. This error, therefore, as would be expected affects more than the d.c. term in the amplitude spectrum.

With the apparent shortcomings in this design and a much greater depth of understanding in this field of research, efforts were made to further develop new techniques and ideas which had evolved over this period.

CHAPTER THREE

SYSTEM IDENTIFICATION

3.1 INTRODUCTION

In the original canceller discussed in the previous chapter the impulse response coefficients were measured directly from the response to an impulse. This method has inherent problems as it is susceptible to noise. In the next canceller the filter coefficients are calculated by correlating the echo path response to a single pseudo random noise sequence, with that sequence. The normal pseudo random binary sequence is modified to provide an essentially flat spectrum of noise over the frequency range of interest. The development of this modified sequence and the function which the response is correlated against is described.

3.2 PSEUDO RANDOM BINARY NOISE

Pseudo random noise is as the name implies, an approximation to true 'white noise'. It is easily generated in a binary or 2 level form and its randomness is limited only by the design criteria. In its most simple form it consists of digital shift register, with two of its taps connected by an 'EXCLUSIVE OR' gate back to the input of the shift register as illustrated in Fig. 3.1.

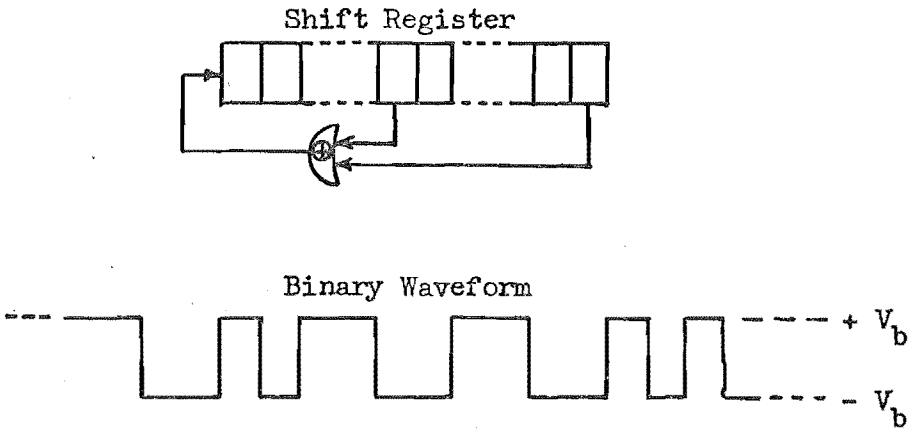


Fig. 3.1 Pseudo Random Binary Sequence Generator and Waveform

The length of the sequence generated from this shift register can be up to $2^N - 1$ clock periods, where N is the number of stages in the register. Dixon[36] gives a detailed account of the properties of various sequences and shows that a maximal length sequence can be generated by using suitable feedback combinations for any length of shift register. A maximal length sequence is one that does not repeat itself inside the length $2^N - 1$. A mersenne prime sequence is a classification of sequence which supposedly has desirable properties, these sequences being of maximal length whose length $2^N - 1$ is a prime number.

One of the most important properties of pseudo random sequences is their auto-correlation function. As the fourier transform of the auto-correlation of any function gives the

energy or power density spectrum, this provides the power density spectrum for any sequence. Now the auto-correlation function of all maximum length sequences have a common form, and can, therefore, be assessed jointly. The auto-correlation function of a pseudo random binary sequence of length $2^N - 1$ is shown in Fig. 3.2 and compared with the auto-correlation function for true white noise. White noise of course has a completely flat frequency spectrum and a resulting delta function as its auto-correlation function.

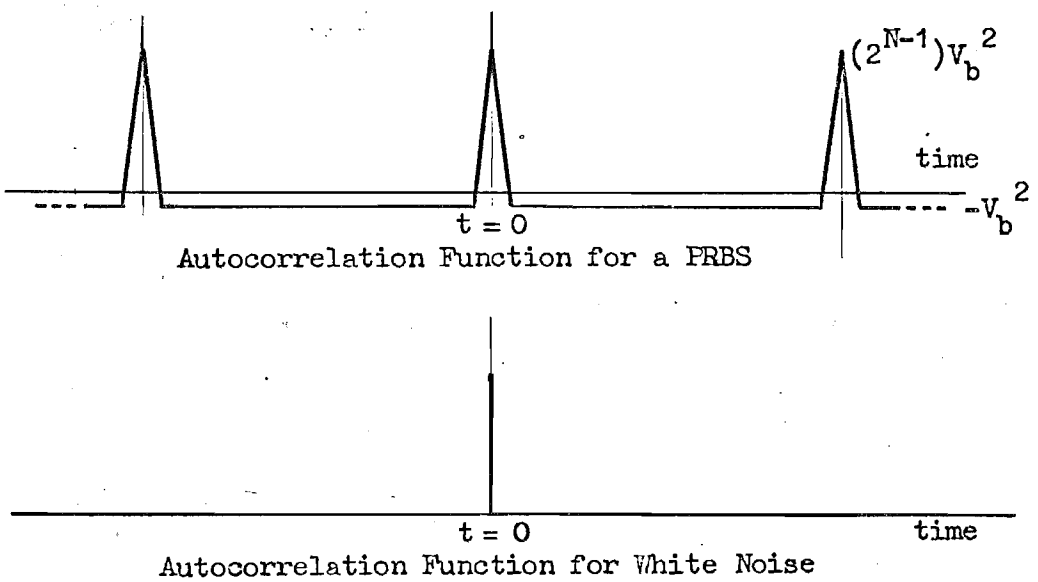


Fig. 3.2 Auto-correlation Functions for a Pseudo Random Binary Sequence and True White Noise

The appropriate function for the pseudo random binary sequence is obtained by correlating a continuous t-sequence with a single cycle of that sequence. The

auto-correlation function itself is repetitive over a period of $(2^N - 1)T$ and is of a triangular nature at the point of maximum correlation. This is an approximation to the delta function obtained from the auto-correlation of true white noise. As N increases and T decreases this approximation will become closer as the amplitude at the point of maximum correlation becomes higher and the width of the triangular function narrows. As N increases the distance between points of maximum correlation will also increase and the spectral lines of the amplitude spectrum will become closer until at the limit where N approaches infinity the spectrum becomes continuous. Two examples at both extremes are:

(i) where N = 89, $1/T = 10^6$ bits/sec, and the sequence period is 1.95×10^9 years.

(ii) where N = 5, $1/T = 10^6$ bit/sec, and the sequence period is 31 microseconds.

Another important property of the PRBS is the bandwidth of the noise when it is being used as a probing signal to establish the transfer function of some system. It is important that the transmitted signal have a relatively flat spectrum over the bandwidth of the system of interest. Otherwise the resultant spectrum that is calculated will be assumed to be coloured by the system where in fact it was a function of the transmitted signal. As already stated the power density spectrum is given by the fourier transform of the auto-correlation function with this being illustrated in Fig. 3.3 with the envelope only being a function of the clock rate.

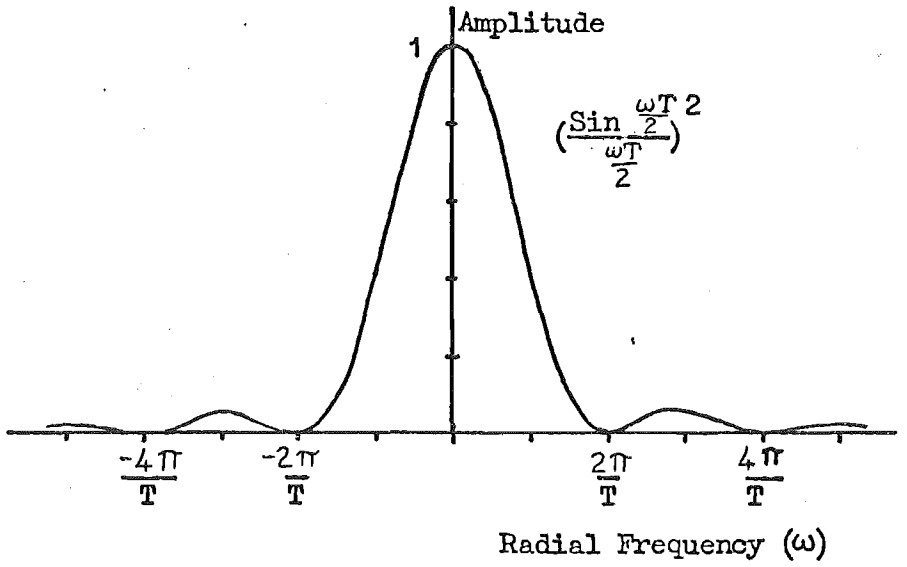


Fig. 3.3 Envelope of the Power Density Spectrum for a Pseudo Random Binary Sequence

The above diagram shows the envelope of the power density spectrum. However, as the sequence is repetitive this spectrum should contain spectral lines spaced by a frequency $1/(2^N - 1)T$ Hz. Only in the case of transmitting one cycle of the sequence will the spectral lines be eliminated.

A further consideration necessary is the effect of correlating a single cycle of the sequence with itself. The result of this process is important in later consideration of the use of a single cycle of the sequence for channel identification. The correlation function shown in Fig. 3.2 is only obtained when a continuous sequence is correlated with a single sequence. The auto-correlation of the single cycle of the sequence has a maximum correlation for zero shift but does not have

a constant correlation for all other shifts as in the previous case. An example of this for a 1023 length sequence is shown in Fig. 3.4 below for a shift of +/- 256.

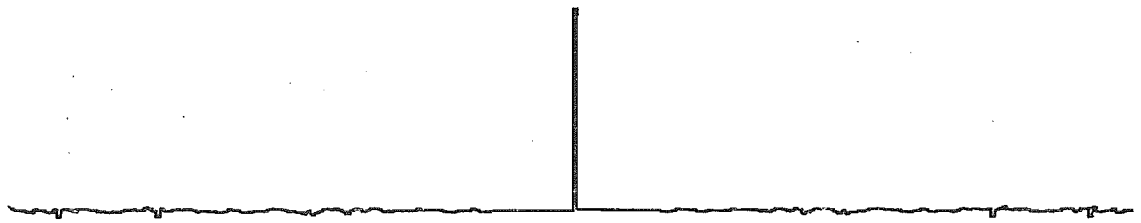


Fig. 3.4 Auto-correlation Function for One Cycle of a 1023 Length Pseudo Random Sequence

3.3 TRI-LEVEL SEQUENCE

The development of the 3 level sequence resulted from the requirement to provide a flatter energy density spectrum over the frequency range of interest. With a sampling rate of 8 KHz (T=125 uS) the amplitude of the energy density spectrum is down to 2.11 dB below its maximum at 3 KHz. This is a result of the $(\sin x/x)^2$ envelope discussed earlier. This does not provide a satisfactory spectrum of noise to determine channel characteristcs over the 0 - 3 KHz frequency range. It will be illustrated later that the sequence must be assumed to be flat over the range of interest for this system identification technique to be valid. If the binary sequence was used to determine the filter coefficients the error at 3 KHz due to the shape of the

spectrum, would mean that the amplitude of components at 3 KHz would be 2.11 dB lower than the correct value. The resultant 38% error means a reduction in echo return loss enhancement of 4.15 dB. A diagram showing the difference between true and measured spectrum using the binary sequence is given in Fig. 3.5.

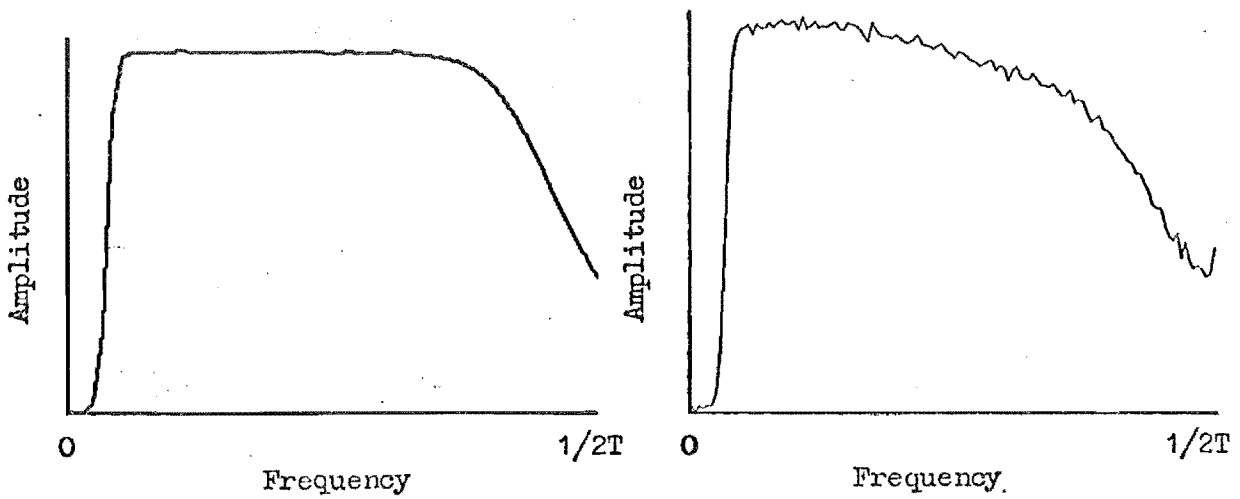


Fig. 3.5 Amplitude Spectrum of a Filter and the Measured Spectrum Obtained Using a Pseudo Random Binary Sequence

The normal method of overcoming this problem is to increase the clock rate thus extending the frequency range of the noise. The consequence of adopting this alternative would be the need either to increase the length of the required sequence, response storage and computation, or to increase the R.M.S. value of the transmitted sequence. For these reasons a new approach was taken which resulted in a sequence of the same length with no extra storage or

computation required. As the resultant impulse response coefficients are only required for a 300 - 3300 Hz system it is not necessary to use a faster clock rate for the transmitted sequence than 8 KHz. This also applies to the required samples of the response.

A pseudo random binary sequence clocked at 8 KHz was modified so as the original sequence was used to determine the polarity of an impulse which was transmitted at an 8 KHz rate. The basic principle of this transmitted signal is shown in Fig. 3.6.

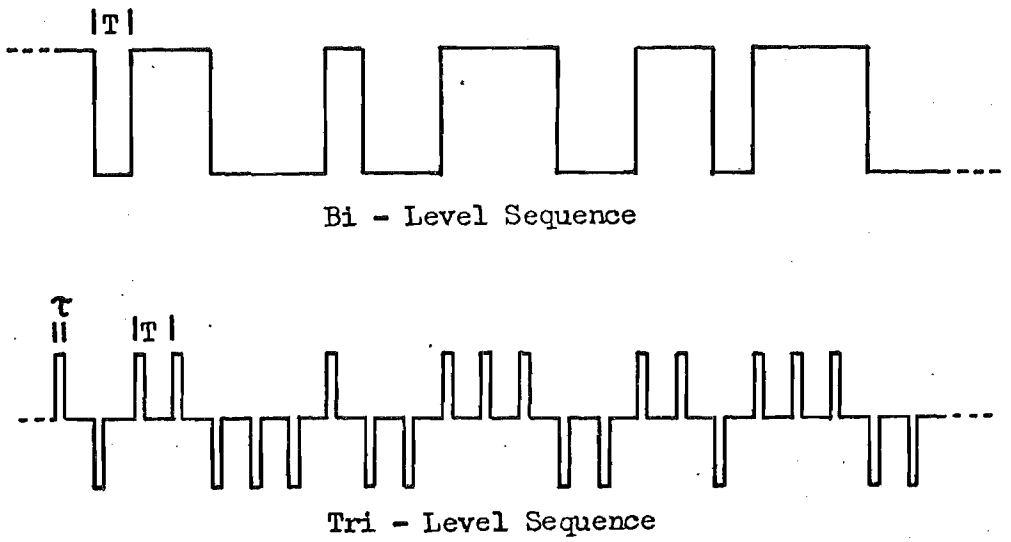


Fig. 3.6 Waveforms of the Two Level and Three Level Pseudo Random Noise Sequences

The effect of this modification is to extend the power density spectrum so instead of the first zero being at f = 1/T, it now occurs at 1/τ effectively scaling the

frequency axis by T/τ. Once again the fourier transform of the auto-correlation function provides the power density spectrum as shown in Fig. 3.7.

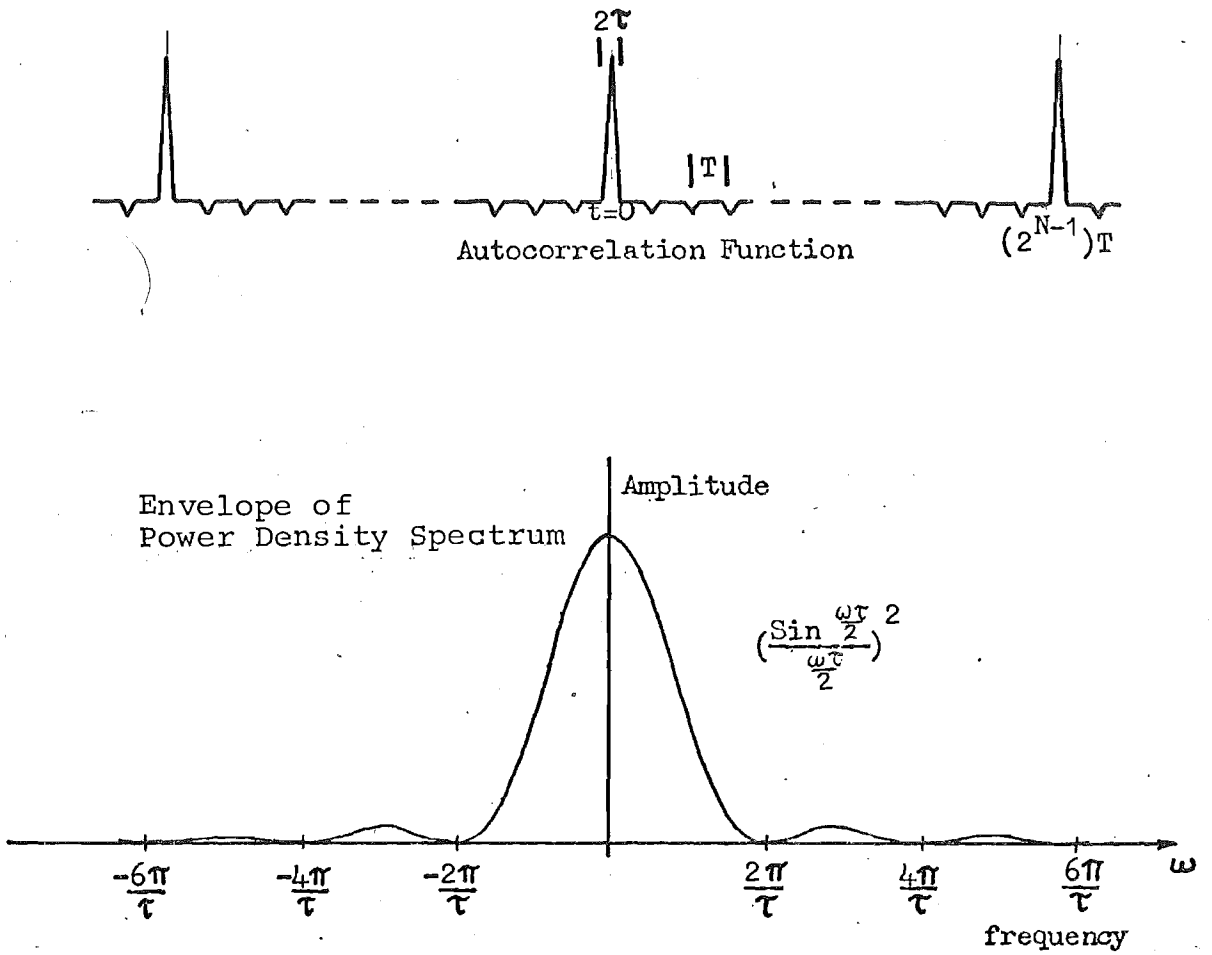


Fig. 3.7 Auto-correlation Function of Tri-level Sequence and Envelope of Power Density Spectrum

3.3.1 Limiting Case of Tri-level Sequence

To substantiate the above statements on the resultant spectrum it is easiest to consider the resultant waveform of the tri-level sequence as a sampled version of the original binary sequence as shown in Fig. 3.5. This sampling process in the limit as τ approaches zero involves multiplying the

sequence by a train of delta functions. In the frequency domain this corresponds to convolving the amplitude spectrum $\sin(\omega T/2)/(\omega T/2)$ with the amplitude spectrum of the sampling function. The illustration in Fig. 3.8 shows the limiting case as $\tau \to 0$. The new auto-correlation function can be easily analysed in the frequency domain by studying the two components of this function individually. The two component waveforms are both trains of delta functions, one having a period PT and the other a period T, where P is the length of the sequence and T is the clock period. When the associated spectrums are summed together the resultant spectrum is flat except for the spectral components at multiples of the clock rate 1/T and the d.c. term as all other components appear in the first component function only. As the power density spectrum is flat over this range so too is the amplitude spectrum.

3.3.2 General Case of Tri-level Sequence

The general case of the tri-level sequence where the width of the impulses is not zero can be easily developed from the above case. If the train of bi-polar delta functions is convolved with a singular rectangular function of length τ as illustrated in Fig. 3.9, then the train of rectangular, randomly polarised pulses to be used as the tri-level pseudo random noise will be achieved.

The resultant amplitude spectrum of $f_1(t)*f_2(t)$ is simply the product of the fourier transforms of the two functions by the convolution theorem - see Appendix II. The resultant spectrum obtained from this product is shown in Fig. 3.10.

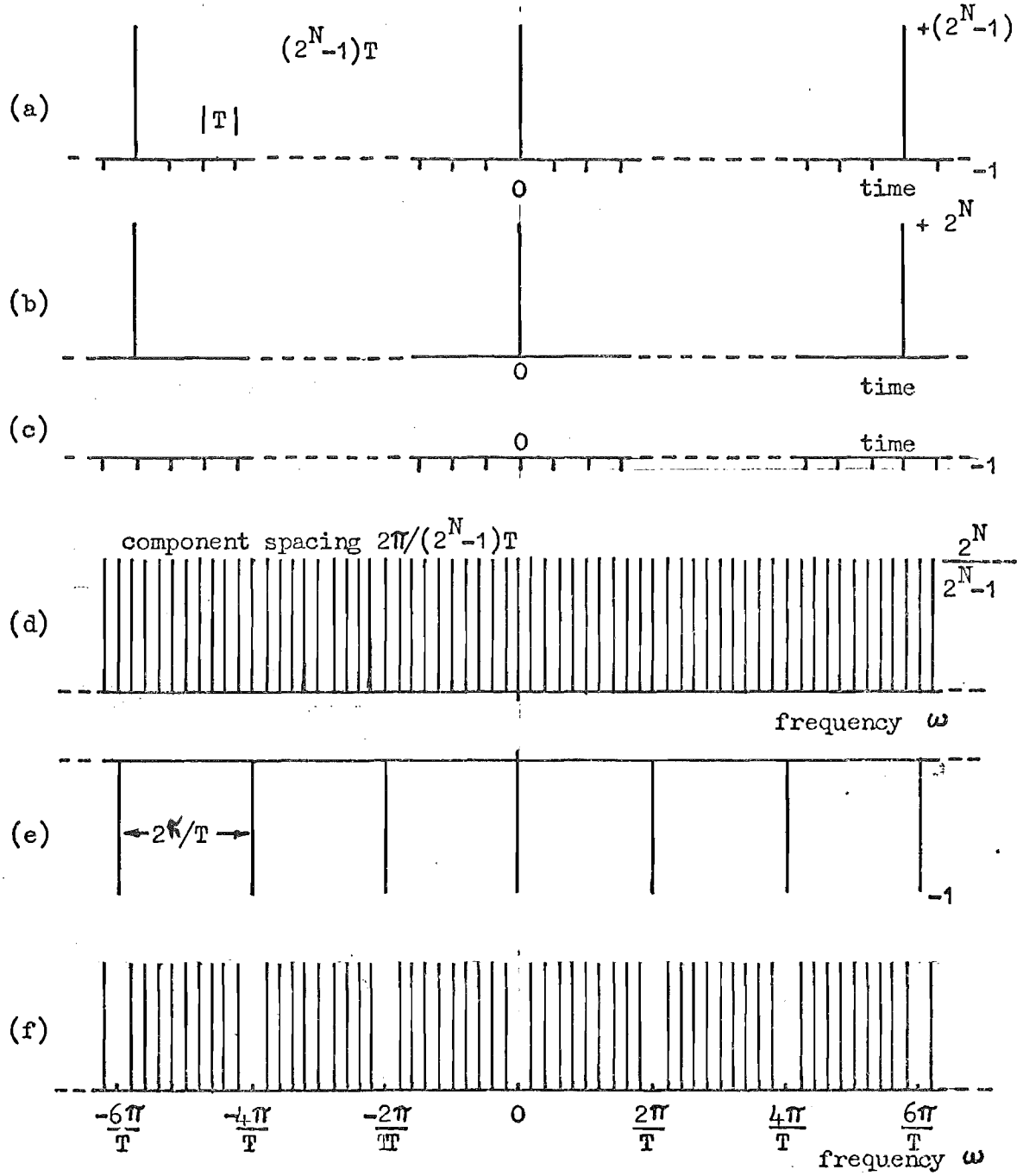


Fig. 3.8 Components of the Auto-correlation Function and its Spectrum of a Tri-level Sequence as $\tau \to 0$.

(a) Auto-correlation function.

(b) Component of (a).

(c) Component of (a).

(d) Spectrum of (b).

(e) Spectrum of (e).

(f) Spectrum of Auto-correlation function (a).

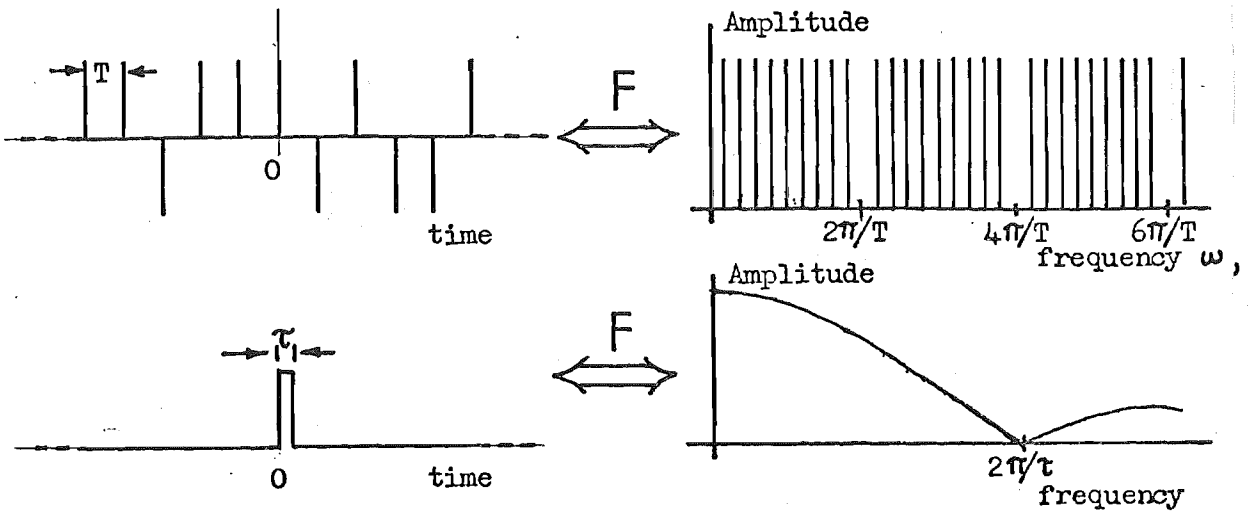


Fig. 3.9 Modification of Spectrum for $\tau \neq 0$

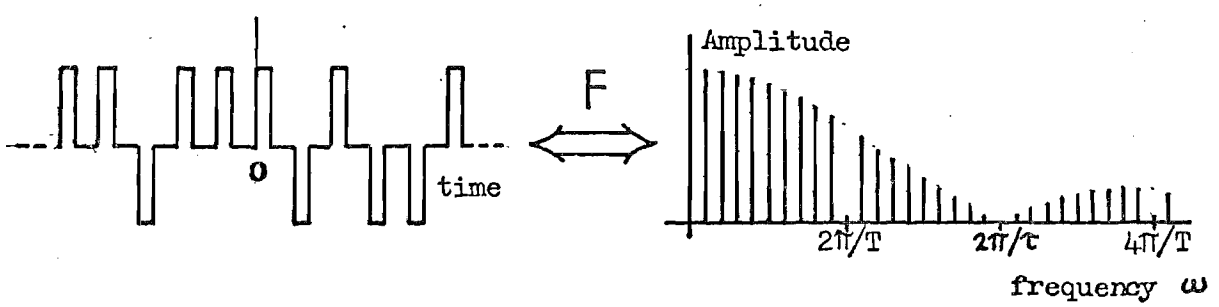


Fig. 3.10 Spectrum of General Case of Tri-level Sequence

It is now clear that by modifying the binary sequence in this manner and reducing τ sufficiently the spectrum of the generated noise can be made to more closely approximate white noise.

3.4 PSEUDO RANDOM NOISE FOR SYSTEM IDENTIFICATION

It is possible to determine the time domain characteristics of a communication channel either directly in the time domain or by transforming data obtained in the frequency domain. If the time domain characteristics only are required it is faster to measure these directly.

On a noise free channel this can take the form of recording the response to a single impulse, thus gaining the impulse response as was the case in the earlier canceller. However, on real systems with noise present some form of averaging is required. The pseudo random binary sequence is a very convenient interrogation signal for averaging.

The time domain response is given directly by the cross correlation of the channel response to an interrogation signal, with the interrogation signal itself, the proviso being that the interrogation signal has the characteristics of white noise over the frequency range of interest. A pseudo random binary sequence carefully chosen can satisfy this requirement.

The application of this technique is direct. By transmitting such a sequence and correlating it with the echo received from the circuit the impulse response of the echo path will result. The result of this discrete correlation also provides the coefficients required for the digital transversal filter which generates a replica of the expected echo.

3.5 CHOICE OF INTERROGATION SIGNAL

As the echo canceller is a discrete time device the clock rate of the sequence generator is required to be a multiple or sub-multiple of the predetermined 8 KHz clock rate. The other requirement of the sequence is that it have an essentially flat amplitude spectrum over the frequency range of interest.

The normal pseudo random binary sequence is characterised by its length 'P', repetition rate 1/PT and clock period 'T'. These factors determine the amplitude spectrum and spectral component spacing. The envelope of the amplitude spectrum is weighted by the fourier transform of a rectangular function in the time domain of length 'T'. This would give around 3 dB 'roll-off' at 3.3 KHz for an 8 KHz clock rate. The other limitation is the phase characteristics over the frequency range which results in a linear phase delay, corresponding to a constant time delay of T/2. As already explained these properties are clearer when the transform of the auto-correlation function are studied. The auto-correlation function for white noise is a true Dirac Delta function whereas the auto-correlation function for the PRBS is the triangular function of width 2T, being repetitive over a period PT. A comparison of these functions and their associated amplitude spectrums was shown in Fig. 3.2.

To satisfy the first requirement of a flat amplitude spectrum the clock rate for a PRBS generator must be much

greater than 8 KHz. To ensure that the sequence appears as noise to the subscriber and not as a tone the repetition rate must not be greater than a few Hz. These requirements lead to choice of a very long sequence length in the order of $1x10^6$. However, it is possible to use a much shorter sequence by modifying it to the three level sequence as described in Section 3.3 and illustrated again here in Fig. 3.11. This eliminates the need for a faster clock rate and hence the need to increase the sequence length. The need to have a long sequence length to overcome the high repetition rate appearing as a tone to the subscriber is also overcome by transmitting only one cycle of the sequence. The truncation of the transmitted sequence to only one complete cycle results in some complication in the correlation process as will become clear.

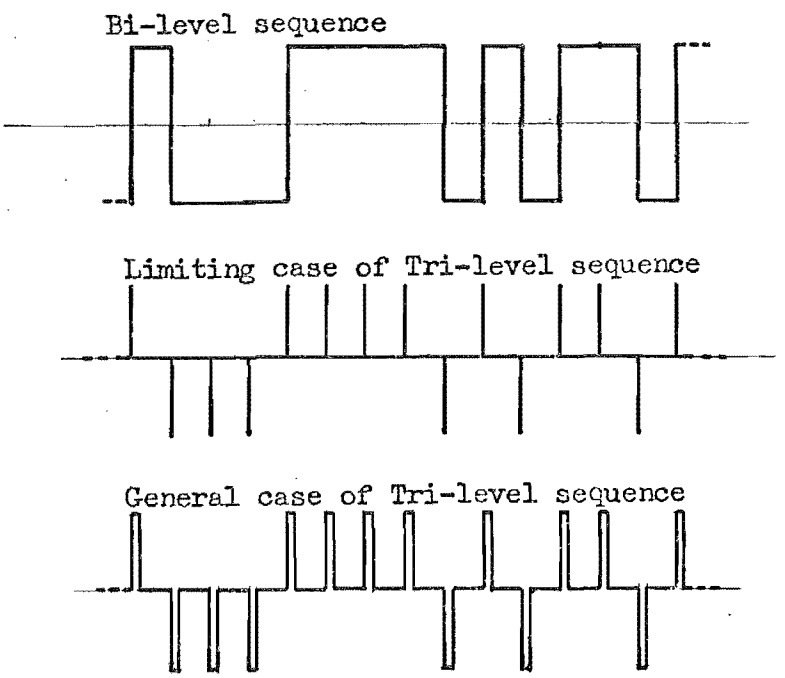


Fig. 3.11 Modification of Bi-level Sequence to Generate a Tri-level Sequence.

3.6 THE TRUNCATED PSEUDO RANDOM NOISE SEQUENCE

To avoid a continuous transmission of the sequence which would mean continuous noise on the circuit and a continuous correlation of the response and sequence, the transmission is truncated to a single cycle of the sequence. The auto-correlation function of a single sequence, however, is no longer represented by the clean rectangular function as explained earlier. A portion of this function was shown in Fig. 3.4. This requires a modification to the function with which the response is correlated, this function being an extended version of that which is transmitted. This will be shown to overcome this problem.

As the impulse response is required to be known for a digital transversal filter, only values at discrete time intervals spaced 'T' apart are required, where 1/T is the clock rate of the discrete system. Furthermore, these will be calculated from the systems response sampled at intervals of T. All correlations and convolutions will be discrete time processes.

Let s(kT) be a discrete representation of the interrogation signal, being one cycle of a pseudo random tri-level sequence of length P, i.e. s(kT) is non zero only for $0 \leqslant k \leqslant P$, and the discrete impulse response h(kT) be known to exist for $0 \leqslant k \leqslant L$, i.e. h(kT) is non zero only for $0 \leqslant k \leqslant L$.

The response of the echo path to s(kT) is r(kT) and is necessarily confined to time period $0 \leqslant k \leqslant P+L$, i.e. r(kT) is non zero only for $0 \leqslant k \leqslant P+L$.

Now s'(kT) is an extended version of s(kT) such that the cross correlation of these two functions approximates a Dirac Delta function in the manner that the auto-correlation of the pseudo random noise sequence does, over the period of interest.

The discrete response r(kT) is given by the convolution of the transmitted signal s(kT) and the impulse response h(kT) plus any noise (including speech) n(kT) present at the time.

$$r(kT) = \sum_{i=0}^{L} s\{(k-i)T\}h(iT)+n(kT) \qquad (5.1)$$

Now the cross correlation of r(kT) and the function s'(kT) which is required to give δ h(kT), where δ is a constant, is given by:

$$\psi_{s'r}(kT) = \sum_{j=0}^{P+L} s'\{(k+j)T\}r(jT) \qquad (5.2)$$

the summation being over a limited range as r(jT) is non zero only for $0 \leqslant j \leqslant P+L$ as previously explained.

Substituting for r(kT) in (5.2)

$$\psi_{s'r}(kT) = \sum_{j=0}^{P+L} s'\{(k+j)T\}\sum_{i=0}^{L} s\{(j-i)T\}h(iT) + \sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT) \qquad (5.3)$$

Introducing variable $\lambda = j-i$

$$\psi_{s'r}(kT) = \sum_{\lambda=-i}^{P+L-i} s'\{(k+i+\lambda)T\} \sum_{i=0}^{L} s(\lambda T)h(iT)$$

$$+ \sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT)$$

$$= \sum_{i=0}^{L} \psi_{s's}\{(k+i)T\}h(iT) + \psi_{s'n}(kT) \qquad (5.4)$$

where $\psi_{s's}(kT)$ is the cross correlation of the transmitted signal $s(kT)$ and function $s'(kT)$.

$h(iT)$ is the discrete impulse response

$\psi_{s'n}(kT)$ is the cross correlation of the function $s'(kT)$ and any system noise $n(kT)$ including speech with a maximum R.M.S. value of -17 dBmo.

substituting $-m = k$ in (5.4)

$$\psi_{s'r}(-mT) = \sum_{i=0}^{L} \psi_{s's}\{(-m+i)T\}h(iT) + \psi_{s'n}(-mT) \qquad (5.5)$$

As $h(mT)$ is known to be non zero only for $0 \leqslant m \leqslant L$

$\psi_{s'r}(-mT)$ is only of interest for $0 \leqslant m \leqslant L$ if

$\psi_{s'r}(-mT) = \delta h(mT)$

and for $\psi_{s'r}(-mT) = \delta h(mT)$

then;

$$\psi_{s'r}(-mT) = \sum_{\substack{i=0 \\ i\neq m}}^{L} \psi_{s's}\{(-m+i)T\}h(iT) + \psi_{s's}(OT)h(mT) + \psi_{s'n}(-mT) \qquad (5.6)$$

where $\psi_{s's}(OT)h(mT)$ is the $\delta h(mT)$ term.

As $\psi_{s's}(OT)$ will always occur in the range $0 \leqslant i \leqslant L$ for any $0 \leqslant m \leqslant L$, now the other two terms must approach zero.

$\psi_{s's}\{(-m+i)T\}h(iT)$ is the auto-correlation error

and $\psi_{s'n}(-mT)$ is the noise error

3.6.1 Minimising Auto-correlation Error

As the discrete impulse response $h(iT)$ is known to be non zero only for $0 \leqslant i \leqslant L$ then $\psi_{s's}\{(-m+i)T\}$ must approach zero for $0 \leqslant i \leqslant L$ and $i = m$ over the range $0 \leqslant m \leqslant L$.

Therefore, $\psi_{s's}\{(-m+i)Y\}$ must approach zero for $(-L+0) \leqslant (-m+i) \leqslant (L-0)$ and $i \neq m$.

therefore, $\psi_{s's}(kT) = 0$ for $-L \leqslant k \leqslant +L$ and $k \neq 0$

now $\psi_{s's}(kT) = \sum_{i=0}^{P} s'\{(k+i)T\}s(iT)$ as $s(iT)$ is non zero only for $0 \leqslant i \leqslant P$

now for $\psi_{s's}(kT)$ to approach zero for $k = 0$ when $s(iT)$ is a pseudo random noise sequence

then $s'\{(k+i)T\}$ must be a shifted version of $s(iT)$ for $k \neq 0$

and $s'\{(k+i)T\}$ must equal $s(iT)$ for $k = 0$

The length of $s'\{(k+i)T\}$ is determined by the range of k and i;

$-L \leqslant k \leqslant +L$ and $0 \leqslant i \leqslant P$

then $s'\{(k+i)T\}$ must be an extended version of $s(kT)$ over the range; $-L \leqslant k+i \leqslant P+L$

now $\delta h(mT) \approx \psi_{s's}(0T)h(mT) = \psi_{s'r}(-mT)$

and $h(mT) \approx (1/\delta)\psi_{s'r}(-mT)$ provided s'(kT) is an extended version of s(kT) for $-L \leqslant k \leqslant P+L$

therefore $$h(mT) = (1/\delta)\sum_{i=0}^{P+L} s'\{(-m+i)T\}r(iT)$$

The sequence s'(kT) is, therefore, an extended version of s(kT) in the positive and negative directions of length L. A diagram showing all of these functions as modelled for the pseudo random binary sequence are shown in Fig. 3.12. The response to the sequence r(kT) was the actual response read from the memory of the canceller using these principles for obtaining the filter coefficients. The effect of auto-correlating the single cycle of the sequence without any extension results in the function $\psi_{ss}(kT)$, and the advantage of correlating the response with the extended sequence s'(kT) instead of s(kT) are obvious. The noise on the scaled impulse response $\psi_{sr}(kT)$ is the noise due to using the unextended sequence for correlation purposes.

If the amplitude of s(kT) is +/- V_s and the amplitude of s'(kT) is $V_{s'}$, the amplitude of the cross correlation function $\psi_{s's}(kT)$ will be $+PV_sV_{s'}$, at k = 0 and $-V_sV_{s'}$, for k non zero and $-L \leqslant k \leqslant +L$. Outside this range the function will have some random value but is out of the range of consideration. The cross correlation function $\psi_{s's}(kT)$ remains only an approximation to a Dirac Delta function even within the range of interest as it is non zero when k is non zero.

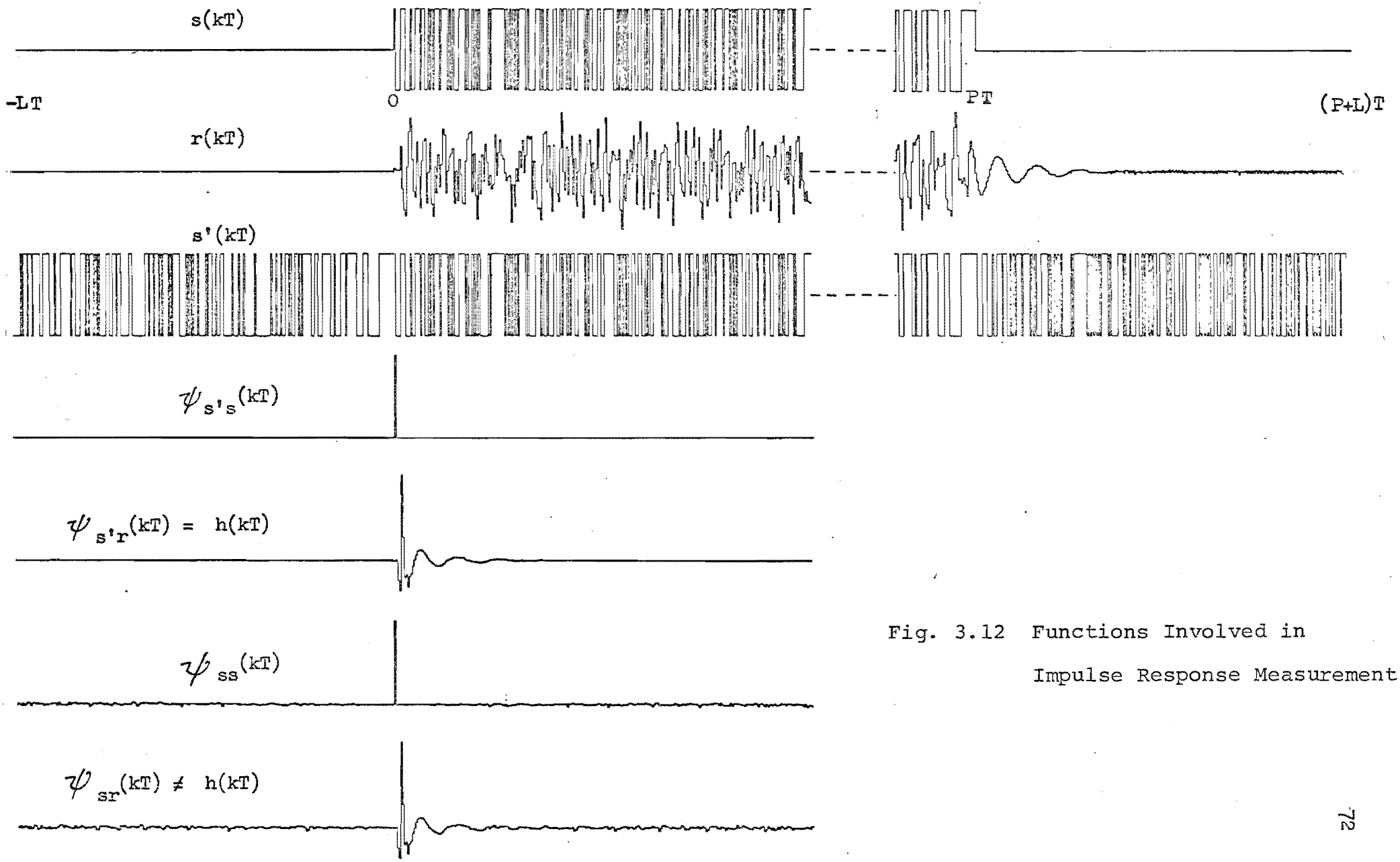


Fig. 3.12 Functions Involved in Impulse Response Measurement

3.7 QUANTITATIVE ERROR ANALYSIS

To analyse errors due to the noise term $\psi_{s'n}(-kT)$, and the imperfect cross correlation function $\psi_{s's}(kT)$ in its approximation to the Dirac Delta function, a statistical approach is used. The appropriate rules are governed by the distribution of means of a sampled population.

If a population has a mean of zero and a standard deviation of σ_1 then the distribution of means of N samples of the population is a normal distribution. Moreover the mean of this distribution is zero and its standard deviation is $\sigma_2 = \sigma_1/\sqrt{N}$.

Now the standard deviation is nothing but the R.M.S. value of the distribution.

The distribution of instantaneous amplitudes of a speech waveform on a telephone circuit was found by Dahlgaard[33] to have a mean of zero and an R.M.S. value of - 17 dBmo or - 20 dB relative to the maximum amplitude expected which is + 3 dBmO.

By using the cross correlation function $\psi_{s'r}(kT)$ as a measure of the impulse response $\delta h(kT)$ there are inherent errors due to the assumption that $\psi_{s's}(kT)$ is a delta function and that the cross correlation of $s'(kT)$ and $n(kT)$ i.e. $\psi_{s'n}(kT)$ will be zero.

$$\text{now } \psi_{s'r}(kT) = \psi_{s's}\{(k+i)T\}h(iT) + \sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT) \qquad (5.7)$$

but $\psi_{s's}\{(k+i)T\} = PV_sV_{s'}$ at $k = i$ and $-V_sV_{s'}$ at $k \neq i$

$$\text{therefore } \psi_{s'r}(kT) = PV_sV_{s'}h(kT) - V_sV_{s'}\sum_{\substack{i=0\\ i\neq k}}^{L} h(iT) + \sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT) \qquad (5.8)$$

The first term is the required result with $PV_sV_{s'} = \delta$, and the final two terms are the errors due to imperfect cross correlation function $\psi_{s's}(kT)$ and the noise term $n(kT)$.

Rearranging (5.8)

$$h(kT) = \frac{\psi_{s'r}(kT)}{PV_sV_{s'}} + \frac{1}{P}\sum_{\substack{i=0\\ i\neq k}}^{L} h(iT) - \frac{1}{PV_sV_{s'}}\sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT) \qquad (5.9)$$

the second term being the cross correlation error and the last term being the error term due to noise or speech.

3.7.1 Cross Correlation Error

This error is given by the term;

$$\frac{1}{P}\sum_{\substack{i=0\\ i\neq k}}^{L} h(iT) = \frac{1}{P}\{\sum_{i=0}^{L} h(iT) - h(kT)\}$$

Now the term $(1/P)h(kT)$ is $20\log(1/P)$ relative to $h(kT)$. For a sequence length of 1023 this error is -60 dB. This is very small for this length sequence. The other error term $(1/P)\sum_{i=0}^{L} h(iT)$ must also be considered.

This term can be considered as the sum of L samples of an infinite population whose mean is zero and standard deviation σ_{h2}. Now the R.M.S. value of the mean distribution of samples will be $\sigma_{h2} = \sigma_{h1}/\sqrt{L}$. The sum of L samples will mean an increase in mean square power of L times and the R.M.S. value will be $L \times \sigma_{h2} = \sigma_{h1}$. So the sum of L samples will have an R.M.S. value equal to that of the impulse response. However, this summation is then scaled by 1/P or - 60 dB. As this represents the error for one coefficient only, this error power will increase by 256 times or 24 dB for the full 256 coefficients. This, therefore, means that the error is 36 dB below the R.M.S. value of the impulse response and, therefore, represents a noise to signal ratio of - 36 dB. This is one limitation on the degree of accuracy to which an echo estimate can be made and gives a limit to echo return loss enhancement. This is for the chosen sequence length of 1023, being one reason for the choice of this length.

3.7.2 Noise Error

This error term is;

$$\frac{1}{PV_sV_s}\sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT)$$

now $V_sV_{s'} = 1$ for $h(kT) = (1/P)\ \psi_{s'r}(kT)$

$$\text{therefore error} = \frac{1}{P}\sum_{j=0}^{P+L} s'\{(k+j)T\}n(jT)$$

During active speech the R.M.S. value σ_{1n} of the instantaneous amplitude distribution of speech is - 17 dBmO. The R.M.S. or σ_{2n} of the distribution of means of P + L samples of n(kT) is, therefore, $\sigma_{2n} = \sigma_{1n}/P+L$ and the sum of P+L samples will be P+L x $\sigma_{2n} = \sigma_{1n}$. This is then reduced by the factor 1/P (-60 dB) to -77 dBmO for P = 1023. Again this error is increased by 256 for the total contribution of all coefficients which raises the error to - 53 dBmO. This error is absolute and not related to impulse response amplitude, but represents the worst case when active speech is present during transmission of the sequence and measurement of the response.

3.7.3 Colouring of Transmitted Noise Sequence

The error due to using a finite width impulse train has been given in Section 3.3. In the limiting case when $\tau = T$ the reduction in echo return loss enhancement is around 4 dB at 3.3 KHz.

3.7.4 Total Error

The effect of these errors is a noise contribution restricting the accuracy of cancellation. The maximum echo return loss enhancement possible after considering the inaccuracies of the filter coefficients alone is 36 dB. The error due to the colouring of the noise sequence can be neglected for $\tau << T$.

CHAPTER FOUR

TRUE LOGARITHMIC COMPANDING

4.1 INTRODUCTION

Companding literally means to compress and expand. It essentially limits the dynamic range of amplitudes to utilise a communication channel more efficiently, by enhancing the level of lower amplitudes. There are two types of companding. Instantaneous companding refers to the instantaneous compression and expansion according to fixed laws and is normally associated with Pulse Code Modulated (PCM) systems. Syllabic companding refers to the application of a fast automatic gain adjustment to raise the mean level of lower speech amplitudes relative to system noise.

Instantaneous companding is an integral part of any modern PCM system. It enables more accurate representation of lower amplitudes without the requirement for more discrete levels or bits. The characteristics of speech waveforms are particularly suited to this operation because of the probability distribution of instantaneous amplitudes. The effect of this is to lower the quantising error for lower amplitudes, therefore, tending towards a constant signal to noise ratio in contrast to the constant noise in a linearly

quantised system. The idle noise remains unchanged. The two common companding laws; the μ-law and the A - law codes are an approximation to a logarithmic curve. A true logarithmic law would give a constant signal to noise ratio. The result is, +/- 128 levels are sufficient to represent the speech waveform.

The use of any form of companding in echo canceller design is relatively new but the true logarithmic format used in this canceller has never been reported. Pseudo logarithmic companding using the A - law code was used by Horna[54] but unnecessary errors are introduced when in subsequent processing the samples are used as if they were logarithmically encoded.

A digital compandor is explained here which provides true logarithmic companding through use of a PROM look-up table. This in itself has advantages over analogue realisations because of the stability factor. Digital companding has, however, been used previously but not in this form. The main advantage in the application of this to the echo canceller is in the simplification of finding the product of binary coded numbers.

4.2 SPEECH CHARACTERISTICS

The inherent characteristics of the speech waveform mean that quantising samples into equally spaced levels results in many of the higher levels rarely being encountered whereas the lower levels are much more likely to occur. The R.M.S. value of the speech waveform on a telephone

circuit during active speech is typically - 17 dBmO as found by Dahlgaard[33], or - 20 dB relative to the maximum value to be accommodated. A mathematical model of the instantaneous amplitude distribution of the speech waveform was proposed by Richards[75]. It was found that a gamma distribution given by;

$$P(x) = \frac{k}{2\Gamma(L)} . (kx)^{L-1} . e^{-kx}$$

where $k = \{L(L+1)\}^{0.5}$

$x = v/v_o$

v_o is the rms value

and $\int_0^\infty P(x)\,dx = 0.5$

gave a good mathematical model of the distribution. The parameter L is varied to approximate distributions for different microphones. For a modern high quality telephone microphone a value of L between 0.2 and 0.5 gives a good approximation. When L = 1 the model reduces to the exponential distribution which is often used as a model. A comparison of the gamma distribution as a model with measurements made by Davenport[34] is shown in a plot of his results in Fig. 4.1.

When the instantaneous amplitude probability distribution is plotted against the logarithmic amplitude of the speech samples the advantage of logarithmic encoding becomes clear. This is shown in Fig. 4.2 and shows a much more even spread of probabilities over the amplitude range. Compare this with the plot against the linear scale where

the vast majority of samples are bunched at the lower end and the logarithmic scale is clearly a better scale to have equally spaced levels for quantisation. Of course, the ideal distribution would be one where all levels had equal probability and although this is practical with a digital conversion it does not have the other advantage of arithmetical simplification. So far this has been a heuristic approach to the advantages of using something other than linear quantising but a more rigorous comparison will follow later.

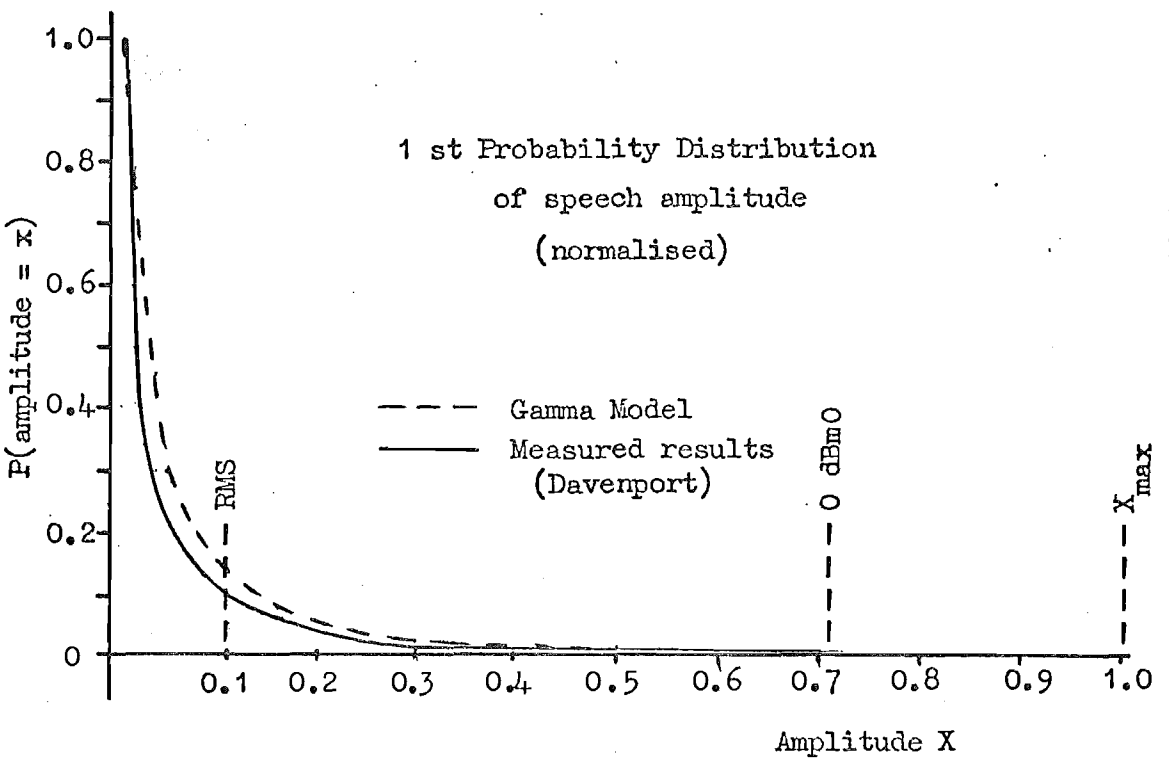


Fig. 4.1 A comparison of actual instantaneous distribution for a speech waveform with a mathematical model using the gamma distribution.

Although the distribution in Fig. 4.2 is plotted against a true logarithmic base this is a non-standard format

compared to other companding curves already used in communications. Two standard companding curves or laws are used in existing communications systems. These are the A - law and the μ - law codes. They are sometimes realised in a piecewise linear form to facilitate the separate treatment of different octaves along the linear amplitude scale for digital conversion. A comparison between the common companding curves and the true logarithmic curve proposed here is shown in Fig. 4.3.

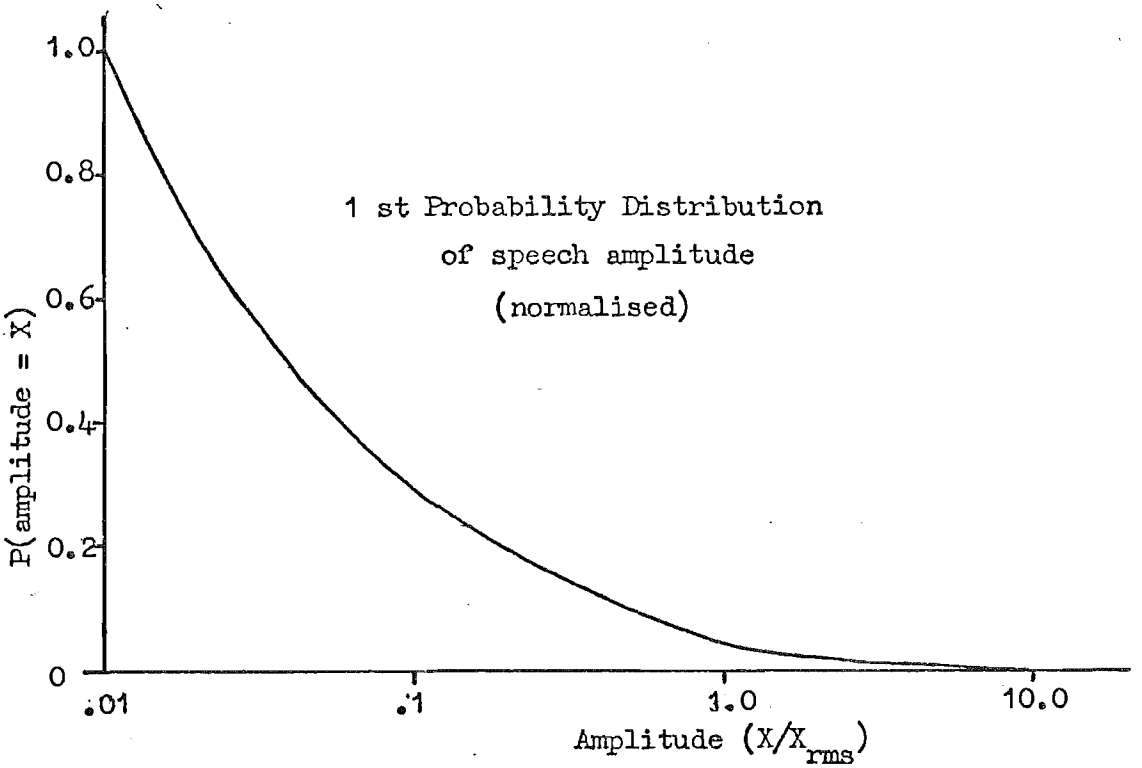


Fig. 4.2 Plot of instantaneous amplitude distribution against logarithmic amplitude scale.

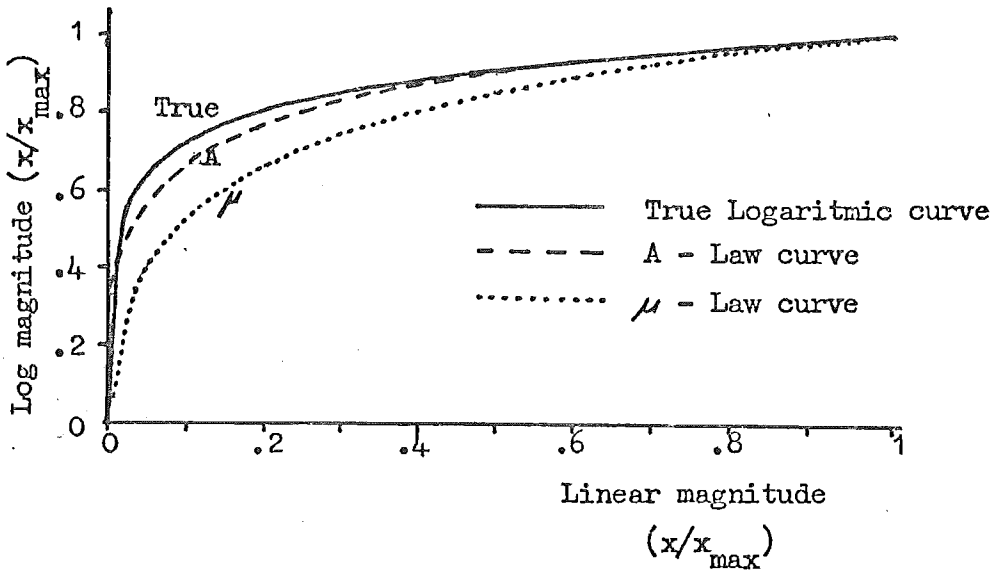


Fig. 4.3 Comparison of Various Compression Curves

4.3 IMPULSE RESPONSE CHARACTERISTICS

The instantaneous amplitude distribution characteristics for the impulse response are less well known. However, results published by the CCITT[12] of tests on the French network revealed a pattern of energy distribution which is used here to approximately determine the instantaneous amplitude distribution for the impulse response. The table of energy distributions published by the CCITT[12] is reproduced in Fig. 4.4.

From these results the impulse response can be modelled as a series of sinusoids of appropriate amplitude for each millisecond period of the impulse response. As the instantaneous amplitude distribution of a sinusoid is well known it was not difficult to establish the distribution for the composite model as shown in Fig. 4.5.

Period in mS.	E_{q1} %	E_{me} %	E_{q3} %
1	79.4	73.3	57.5
2	85.1	81.3	75.8
4	91.2	90.2	93.3
6	97.7	96.6	96.3
8	100	100	100

E_{q1} - Associated with E.T.A.'s below first quartile
E_{me} - " " " " the median
E_{q3} - " " " " third quartile

Fig. 4.4 Impulse Response Energy Distribution Table. Reproduced from Ref. (12)

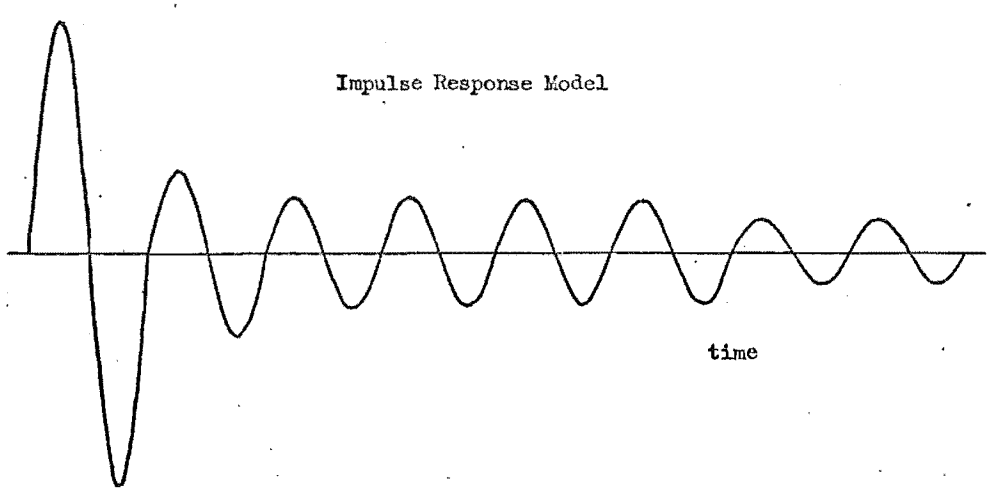


Fig. 4.5 The Model of the Impulse Response

A comparison of the distributions for speech and the impulse response is shown in Fig. 4.6.

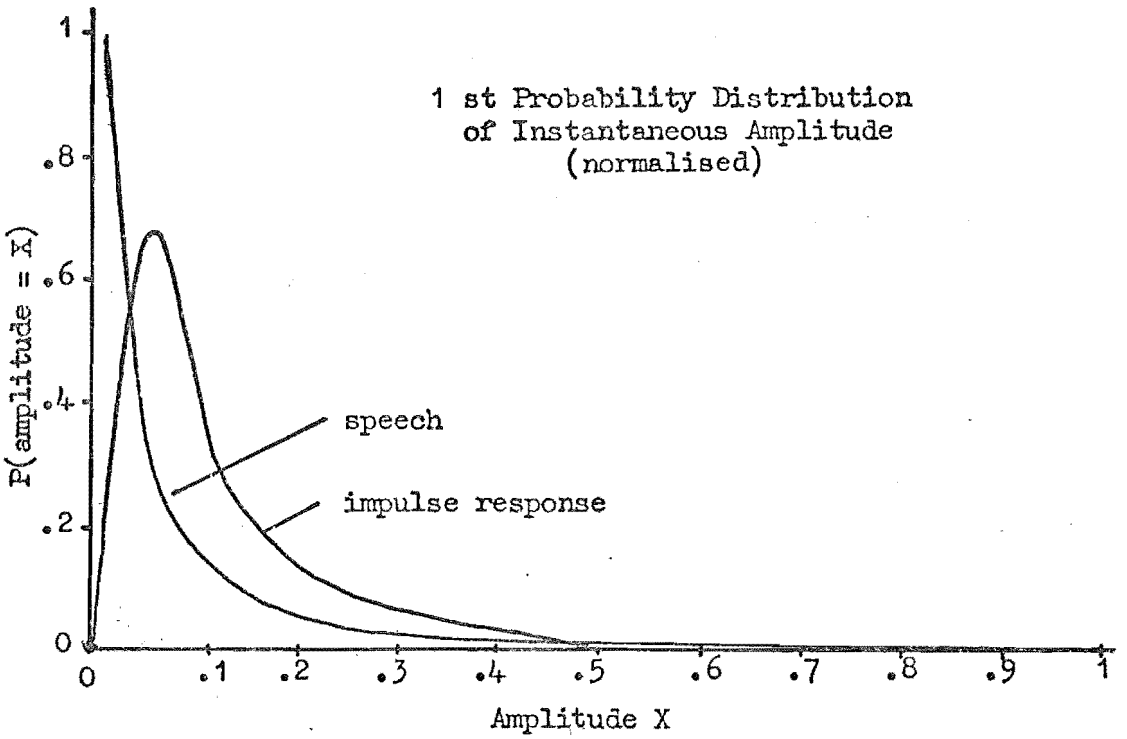


Fig. 4.6 Comparison of the instantaneous amplitude distributions for the speech and impulse response waveforms.

From this model it is clear that for the mean level of echo the impulse response has a similar instantaneous amplitude distribution as that of speech and, therefore, is also suited to a companded format.

4.4 CHOICE OF LOGARITHMIC BASE

According to Halliwell[47] a 12 bit linear and 8 bit companded format provide low enough idle noise and noise to signal ratio. This is based on the necessity to keep the idle noise governed by the linear quantising to a minimum, and to provide the dynamic range which is governed by the

compression curve. The signal to noise ratio during active speech will be shown to be directly related to the number of levels on the compression curve.

As already stated standard compression curves are not logarithmic to overcome the problem of having to find the logarithm of zero. This is one consideration which governs the choice of logarithm base here.

An 11 bit linear magnitude must be converted to only a 7 bit logarithmic magnitude. To overcome the problem of finding the logarithm of zero magnitude the A/D convertor is offset so as there is no zero level. Instead of the linear values then ranging from ½ to 2047+½, these values are considered to range from 1 to 4095 in steps of 2. This overcomes the problem of finding the logarithm of values less than unity and means that the logarithm of the smallest linear value '1' will be zero whatever base is used. This offset and scaling arrangement is shown in Fig. 4.7.

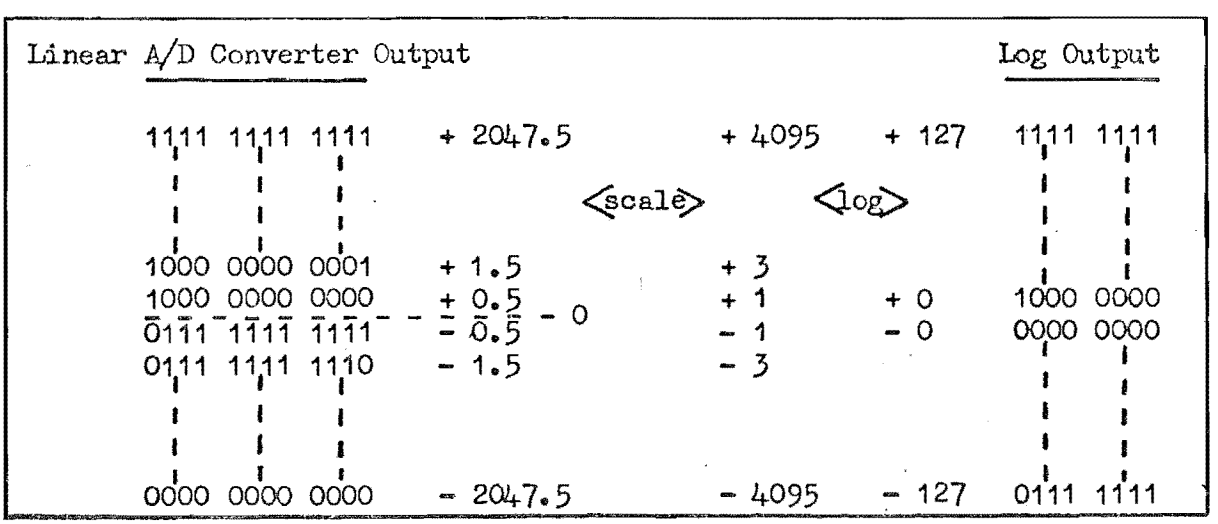


Fig. 4.7 Offsetting, scaling and logarithmic conversion of linear, digital values.

For the full 7 bit logarithmic magnitude to be utilised

$$\log_m(4095) = 127$$

$$\text{and } \log_m(1) = 0$$

$$\text{now } m^{127} = 4095$$

$$\text{therefore } m = (4095)^{1/127} = 1.06768$$

Of course, $\log_m(x)$ is related to $\log_e(x)$ by the factor $1/\log_e(m)$, i.e.

$$\log_m(x) = \log_e(x)/\log_e(m)$$

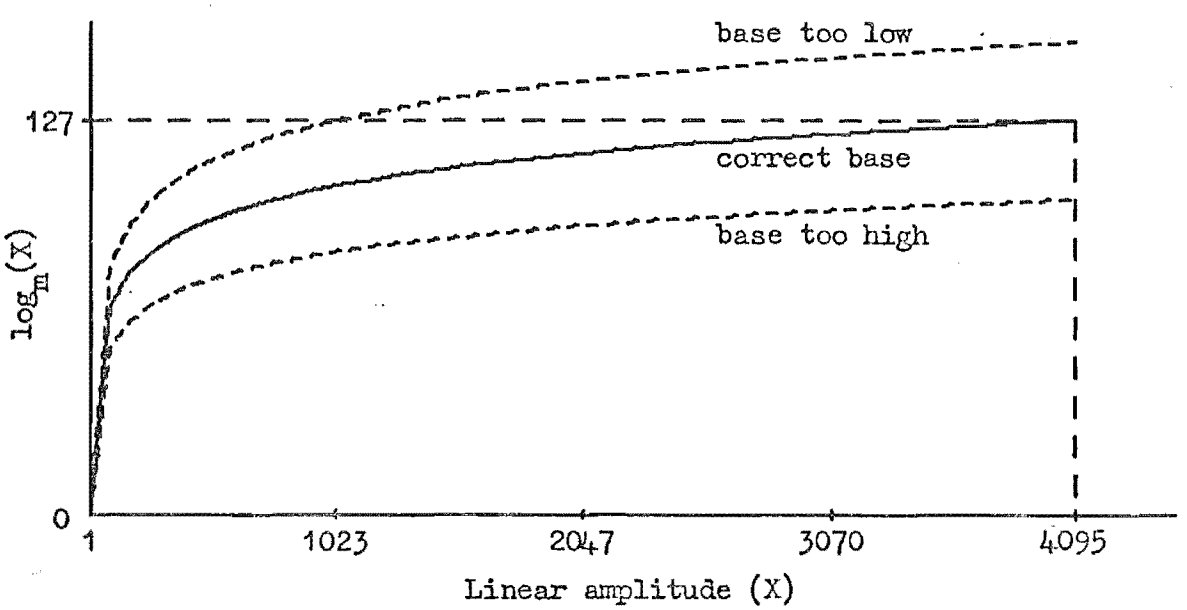


Fig. 4.8 Logarithmic compression curve showing the effect of varying the logarithm base.

The logarithm curve used for companding is shown in Fig. 4.8 and the effect of changing the base is also illustrated. If m is increased not all logarithmic levels are

used and conversely if decreased not all linear levels fall within the range of the logarithmic scale.

4.5 QUANTISATION NOISE

In any system where analogue samples are quantised the errors in assigning a discrete level to samples gives rise to quantisation noise. This noise is proportional to the distance between the discrete levels and consequently inversely proportional to the number of levels. The number of bits used to represent the sample digitally determines the amplitude of this noise.

In linearly quantised system all levels are equally spaced and, therefore, the error or noise generated by the quantising of any sample is constant irrespective of amplitude. The mean error in quantising samples is ¼ of a level. If N is the number of bits in the digital representation, then 2^N is the total number of levels or +/- 2^{N-1} levels. If the mean error is ¼ level then the error noise is $20 \log(1/(4x2^{N-1}))$ below the maximum value to be represented. This noise will be constant irrespective of whether speech is present. For this reason the noise must be kept to a minimum which is usually accepted as -69 dBmO. This requires linear quantisation to 12 bits or +/- 2048 levels.

If on the other hand the amplitude scale is quantised in such a way that the more frequently encountered levels are grouped closer together to reduce errors at these levels this noise error will not be constant. When speech samples

are coded with a μ - law or A - law companding scale only 8 bits or 256 levels are required. This is now an accepted standard for Pulse Code Modulated communications systems.

As already established the quantising error is directly proportional to the difference between adjacent levels or inversely proportional to the slope of the encoding curve. As the slope of the true logarithmic curve is inversely proportional to the amplitude then the error is directly related to the amplitude of the signal. This, therefore, gives a constant signal to noise ratio whereas the linear encoding is limited by the idle noise. The principle behind logarithmic quantising and the associated quantisation noise is illustrated in Fig. 4.9.

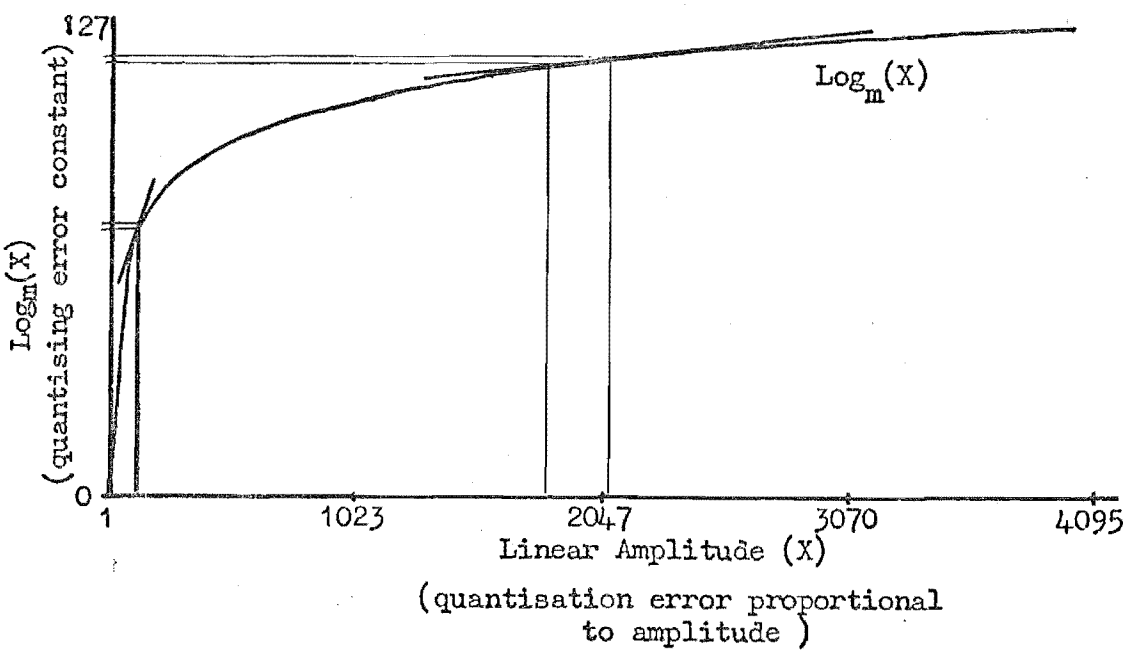


Fig. 4.9 Error Due to Compression Curve

In normal communications applications it is not important that the encoding curve is not truly logarithmic and in fact it is more convenient to use one of the pseudo logarithmic curves mentioned. However, for the purpose of this echo canceller it is important as the logarithm is used to simplify the generation of products in the convolution process. To use a pseudo logarithmic curve as Horna[54] proposed, presumably for the sake of standardisation, is to realise the benefits but to only go halfway in using them. From his error analysis it appears that the approximation meant a loss of 4 dB in echo return loss enhancement compared to what is expected in this system.

The simplification that logarithmic coding enables in the convolution equation is shown.

The linear equation;

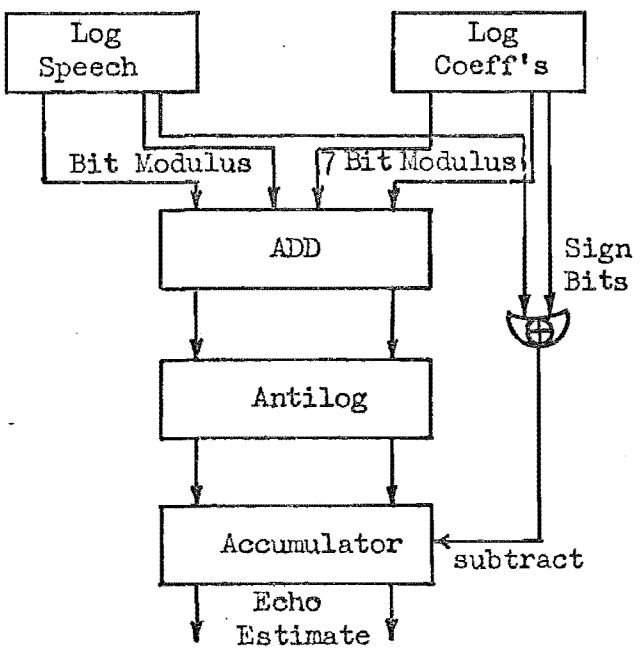
$$e'(kT) = \sum_{i=0}^{255} h(iT)s\{(k-i)T\}$$

reduces to $$e'(kT) = \sum_{i=0}^{255} \text{antilog}\{\log(h(iT)\} + \log\{s((k-i)T))\}$$

4.6 PRACTICAL LOGARITHMIC ENCODING

The coding to a true logarithmic format is simply achieved as a digital conversion. This is done with a Read Only Memory programmed as a logarithmic look-up table. The linearly digitised magnitude of the sample is used to address the look-up table with the output programmed to provide the logarithm of this magnitude. As the magnitude only needs to be converted with the sign bit being carried separately, 11

bit linear and 7 bit logarithmic formats are used. This requires a 2048 x 7 bit Programmable Read Only Memory which becomes very economical when shared over many channels. The antilog PROM need only be 256 x 11 but must be channel dedicated due to its more constant use. The logarithm of each speech sample is obtained when it is first converted to a digital word and both speech samples and filter coefficients are stored in this format. Filter coefficients although calculated as linear values are also converted using the same look-up table. Further details of circuitry are discussed in Chapter 7 and Appendix V. A diagram illustrating the manner in which the convolution equation is realised using the logarithmic form is shown in Fig. 4.10.



$$e'(kT) = \sum_{i=0}^{255} \text{Antilog}(\log(h(iT)) + \log(s(k-i)T))$$

Fig. 4.10 Realisation of Discrete Convolution Using logarithmic Format

4.7 LOGARITHMIC QUANTISATION ERROR

The mean amplitude of the noise due to quantising on the compressed logarithmic scale is as always ¼ of the distance between levels. The slope of the logarithmic scale relative to the linear scale gives the absolute error. An illustration of this and a comparison with common compression curves is shown in Fig. 4.11.

$$\text{now } \frac{d}{dx} \log_m x = \frac{d}{dx}(\log_e x / \log_e m)$$

$$= (1/\log_e m) \times \frac{d}{dx}(\log_e x)$$

$$= 1/(x \log_e m)$$

$$= 15.269/x \quad \text{for } m = 1.0677$$

The mean error is proportional to the reciprocal of the linear scale.

$$\text{mean error} = x/(4 \times 15.269)$$

The error noise is directly proportional to the amplitude x and 20 log(1/61) dB below it. This gives the noise due to logarithmic quantisation as - 36 dB relative to the signal sample, or filter coefficient amplitude.

As this noise error is introduced both to the signal sample and filter coefficient, noises will add giving a resultant of - 33 dB thus setting the upper limit on the

cancellation possible. However, it must be remembered that this is relative to the amplitude of the echo, and sets the maximum possible mean echo return loss enhancement. This does not give the level of idle noise when speech is absent. The idle noise is set by the linear quantisation already discussed.

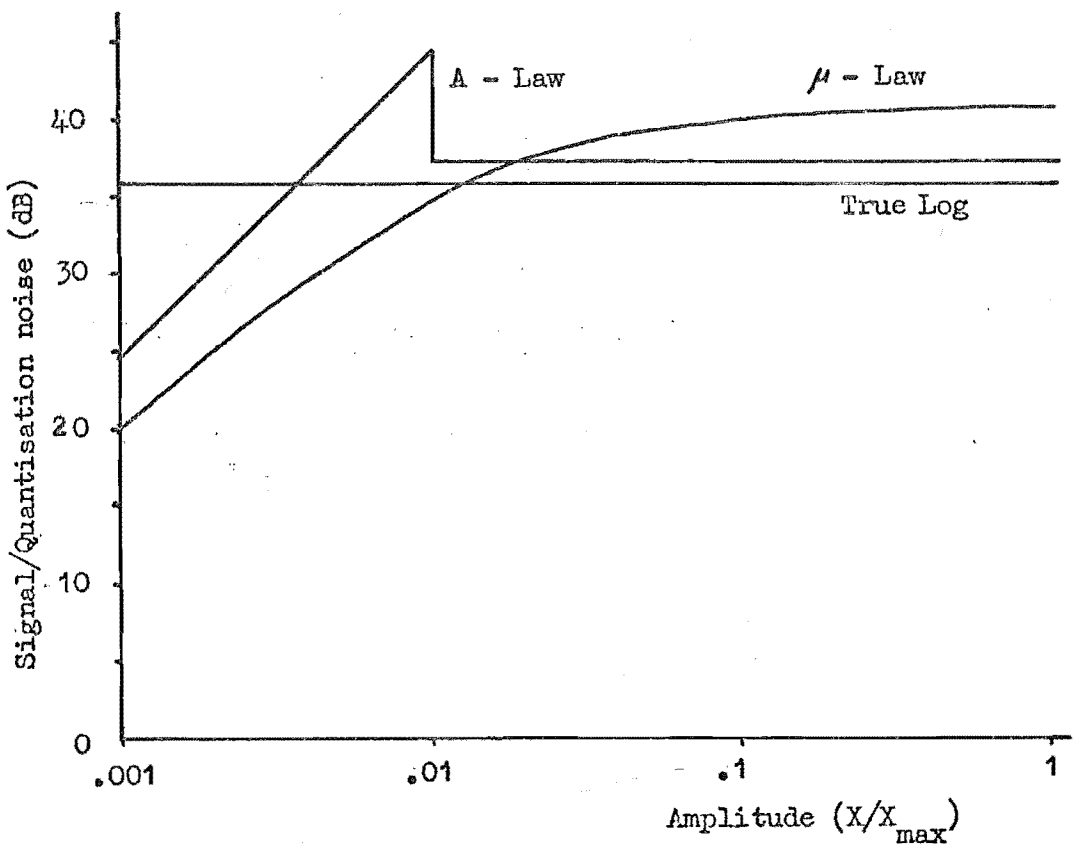


Fig. 4.11 Quantisation Error for Various +/- 128 Level Compression Curves

CHAPTER FIVE

TIME VARIANCE OF ECHO PATH

5.1 INTRODUCTION

Although time variance of echo path characteristics is not a significant problem on New Zealand circuits, consideration has been given to this problem as it is a major factor governing design of echo cancellers elsewhere. The most serious time variant is a continuous and cyclic variation in the phase of the impulse response around the echo path. This is encountered on frequency division multiplexed transmission systems not employing synchronised modulation and demodulation processes. It is proposed here that this predictable time variance be tracked separately to random variations instead of allowing the filter coefficients to clumsily follow this regular variation. Until now this cyclic variation has been tracked as though it was a random variation, using none of the predictability it possesses. There are, however, unpredictable variations with time which must either be adapted to, or be recognised to enable the filter coefficients to be re-established.

After developing the idea of a phase tracking system for tracking cyclic phase variation, and the publication of an article by this author[87] on the design of a

practical Hilbert Transformer suitable for application to this system, Gitlin & Thompson[42] published a comprehensive paper proposing just such a system. This paper confirmed the optimism in such a technique providing a more satisfactory solution to this difficult problem.

5.2 CAUSES OF TIME VARIANCE

Time variance of the echo path characteristics require an effective change of coefficients in the transversal filter to enable it to accurately model the echo path. The rate at which these variations occur has determined the ability of adaptive cancellers to operate satisfactorily. Intermittent variations which occur infrequently are less difficult for adaptive cancellers to adjust to but those which are due to a cyclic phase variation termed 'phase - roll' can prove impossible to follow.

5.2.1 Intermittent Time Variance

This type of time variance is unpredictable and can be caused by many different changes in the transmission path. The switching of transmission paths or the change of a termination at the subscribers end are possible reasons.
The changed termination on the hybrid transformer can be caused by the switching of extensions at the subscribers premises.

This type of variation can easily be accommodated by the adaptive canceller with the coefficients converging to

the correct value in less than 1 second after active speech commences. This solution is quite satisfactory except that the filter cannot adapt to changes unless speech from the distant subscriber is present and there is no double talking. In a non-adaptive canceller as is proposed here, a complete recalibration is required. In the case of the earlier canceller this involved the transmission of an impulse and the measurement of the response. The later canceller requires the transmission of a noise sequence and a correlation process to calculate the coefficients. The correlation process can be completed in 400 mS and is not adversely affected by the presence of speech. However, this would not be satisfactory if these random changes were more regular than about 2 per minute. It is estimated that the changes would occur at an average of less than 1 per minute.

5.2.2 Cyclic Time Variance

Although only a very small portion of national transmission circuits in New Zealand - less than 1% - are subject to this type of time variance, this is a major problem on other national telephone networks. This is particularly so in Australia for instance where only 88% of subscribers in Victoria had no chance of encountered phase roll on international calls. The rate of phase roll is typically less than 2 Hz but can be as great as 5 Hz. The diagram in Fig. 5.1 shows the echo path on which the frequency shift or phase roll is generated.

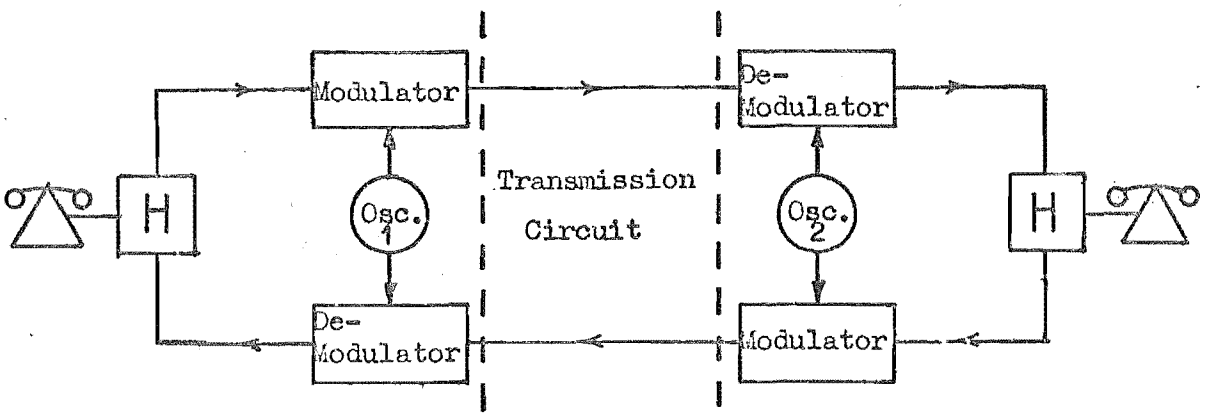


Fig. 5.1 The Echo Path Incorporating Non-synchronised Frequency Division Multiplexing

The frequency shift around the circuit is generated in the modulation and demodulation stages of frequency division multiplexing. The practice of shifting audio frequency channels to higher frequencies is achieved by heterodyning them with submultiples of a master oscillator. If the channel is shifted back to its original place in the spectrum using exactly the same frequency as in the modulation process then no frequency shift occurs. Unfortunately, the modulation and demodulation processes are at different ends of a transmission circuit and, therefore, sometimes use oscillators which are not synchronised. This results in a frequency shift around the echo path which manifests itself in a cyclic variation in the phase of the impulse response.

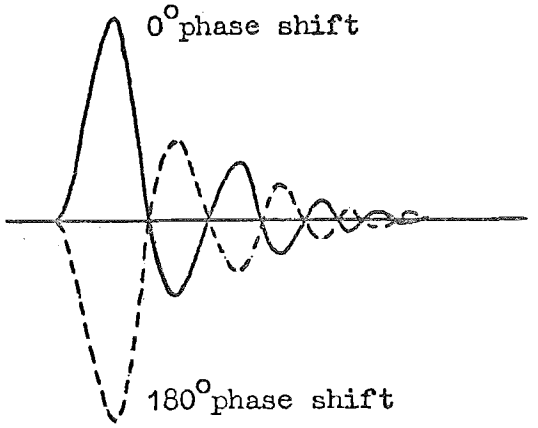


Fig. 5.2 The Effect on the Impulse Response of Cyclic Time Variance

With a phase roll of 2 Hz the impulse response will go through 180° every ¼ second, and will repeat itself every 0.5 seconds. For this reason it is difficult for the conventional adaptive canceller to adapt its coefficients fast enough to follow this rate of change. The adaptation not only must be capable of following at this rate but must remain close enough to provide satisfactory cancellation. A much more satisfactory solution seemed to be to maintain the basic set of coefficients which essentially give the impulse response of the channel at a time say t = 0 and provide a means of varying the phase separately. As this form of time variance provides such a predictable variation in the filter coefficients with them repeating regularly, it was a clumsy adaptation process which required the variation of 64.

filter coefficients where there was essentially only one variable, that of phase. A diagram in Fig. 5.2 shows the simple relationship between impulse response where the phase shift around the circuit has changed by 180° for all frequencies. A constant shift in frequency across the whole spectrum of interest represents a constant phase shift per unit time for all frequencies. The time domain representation of a 180° phase shift on a waveform such as the impulse response is obvious. The relationship for phase shifts between these limits, however, is not so simple.

5.3 COMPENSATING FOR PHASE ROLL

To compensate for phase roll separately the requirement is to apply the frequency shift to the echo estimate which occurs around the real echo path. When the frequency shift is considered as a rate of change of phase this can be translated into varying the impulse response to give a constant change of phase per unit time.

5.3.1 Generating Phase Roll

Phase roll can be achieved by generating an estimate of the echo according to the established filter coefficients along with a quadrature or 90° phase shifted version of this estimate. It is well understood that any phase shift can be generated if two quadrature components of a signal are available. Combining the two components in the correct proportions provides the required phase shift. With the real component scaled by the cosine of the phase shift required

and the quadrature component by the sine, these scaled components are summed to get the required result. This process as it is applied to the echo canceller is illustrated in Fig. 5.3.

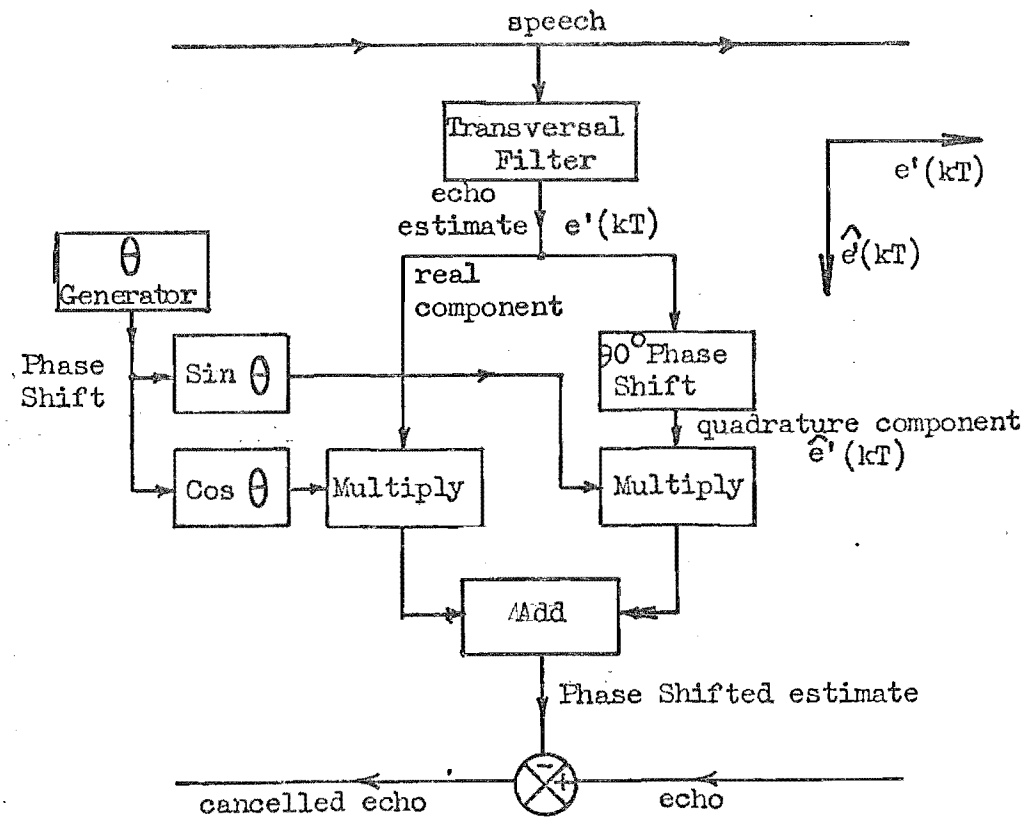


Fig. 5.3 The Generation of Cyclic Phase Shift Using a Quadrature Component

Apart from the intermittent time variances the initially established coefficients can now be used to generate any frequency shift with the rate of phase roll being determined by the rate at which the phase angle θ changes. The generation of the quadrature component is relatively straight forward with a hardware realisation

of the Hilbert Transform provided that some delay in the real component can be accommodated. The application of the Hilbert Transform to this problem is discussed in Chapter 6.

5.3.2 Tracking Phase Roll

One complication is the necessity to generate an error signal in order to 'steer' the change of phase in the required direction. Consider the true echo as a rotating vector $e_r(t)$ being the real component. The vector $e_{r'}(t)$ is the estimate of the vector $e_r(t)$ and until time $t = 0$ has been rotating in phase with it. If a relative phase shift θ occurs between them, say $e_{r'}(t)$ leads $e_r(t)$, the component $e_{c'}(t)$ of $e_{r'}(t)$ gives some degree of cancellation. These relationships are illustrated in Fig. 5.4.

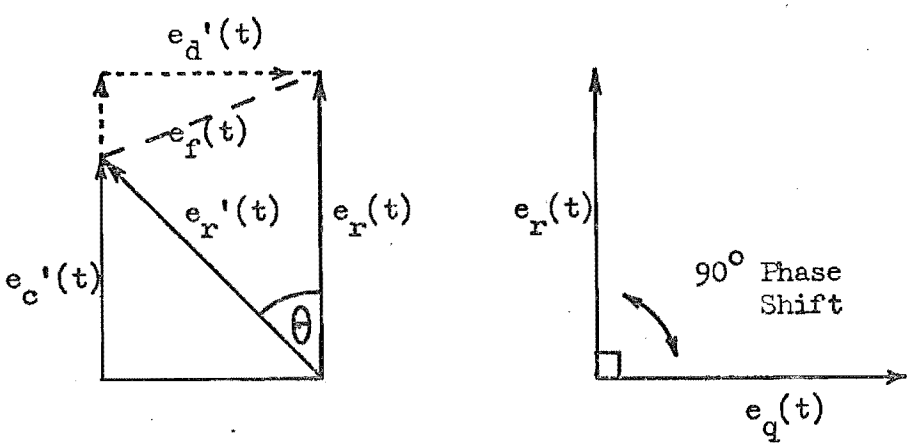


Fig. 5.4 Vectorial Components of the True Echo and its Estimate Under Phase Roll Conditions

The difference vector $e_f(t)$ comprises two components, one of which is in quadrature with $e_r(t)$, i.e. $e_{d'}(t)$. If the quadrature component $e_q(t)$ of $e_r(t)$ is generated as in Fig. 5.4 this will have some correlation with $e_{d'}(t)$. If any correlation does exist then $e_{r'}(t)$ and $e_r(t)$ are no longer in phase. This is irrespective of the magnitude of the two vectors, however, the magnitude of the correlation will depend on the amplitudes. Correlating $e_q(t)$ and $e_{r'}(t)$ will, therefore, give an error signal. The sign of the correlation will indicate the direction in which the phase needs to change. The component of $e_f(t)$ that is in phase with $e_r(t)$ will have no correlation with the quadrature vector $e_q(t)$. A schematic diagram of this error generation process is shown in Fig. 5.5.

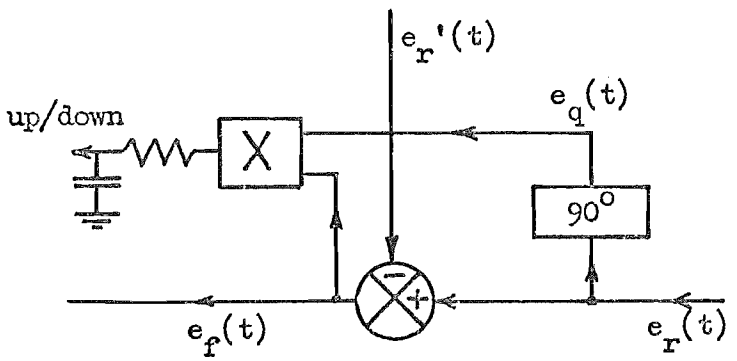


Fig. 5.5 The Generation of an Error Signal

The output of the circuit in Fig. 5.5 gives an error signal which can be used to determine the direction in which the phase is to be shifted. Phase roll is considered in this context to be a rate of change of phase and although the

phase varies rapidly, its first derivative frequency does not. The error signal, therefore, can be integrated as it is slowly varying, thus reducing the susceptibility to false correlations with noise or near subscriber speech. This does limit its ability to initially converge, however, and it is considered preferable, therefore, to have some initial estimate of the rate of change of phase. A means of making an initial estimate from the response to the noise sequence will be discussed in the next section. There is the normal conflict of any control system in this error signal generation of trying to converge quickly yet minimising the effect of noise.

In generating the error signal, the amplitude of component $e_{d'}(t)$ is proportional to the sine of the phase error as will be the amplitude of the resultant correlation. This will vary, however, with amplitude of the speech and to get a true indication of the absolute magnitude of the phase error it may be necessary to scale this error signal by the amplitude of $e_{r'}(t)$. As the amplitude of $e_{d'}(t)$ is proportional to the sine of the angle it increases rapidly as it increases from zero. It reaches 14% of maximum for an 8^{o} phase shift, which represents a phase error resulting in an echo at - 17 dB relative to the amplitude of the echo prior to cancellation. This provides a statistically large component which when correlated (multiplied and integrated) with $e_q(t)$ would give a reliable error signal.

During double talk $e_r(t)$, $e_q(t)$ and $e_f(t)$ will also contain speech from the near end subscriber. However,

components of this speech in $e_f(t)$ and $e_q(t)$ are truly orthogonal and will have no correlation contributing to false phase shifting. The structure of a canceller incorporating such a phase tracking system is shown in Fig. 5.6.

The generation of the sine and cosine functions would be done digitally with Read Only Memory look-up tables and the 90^o phase shift network would be achieved with an analogue tapped delay line used as a Hilbert Transformer. All other circuitry is conventional and needs no discussion except to say that the sine and cosine multipliers are multiplying D/A convertors.

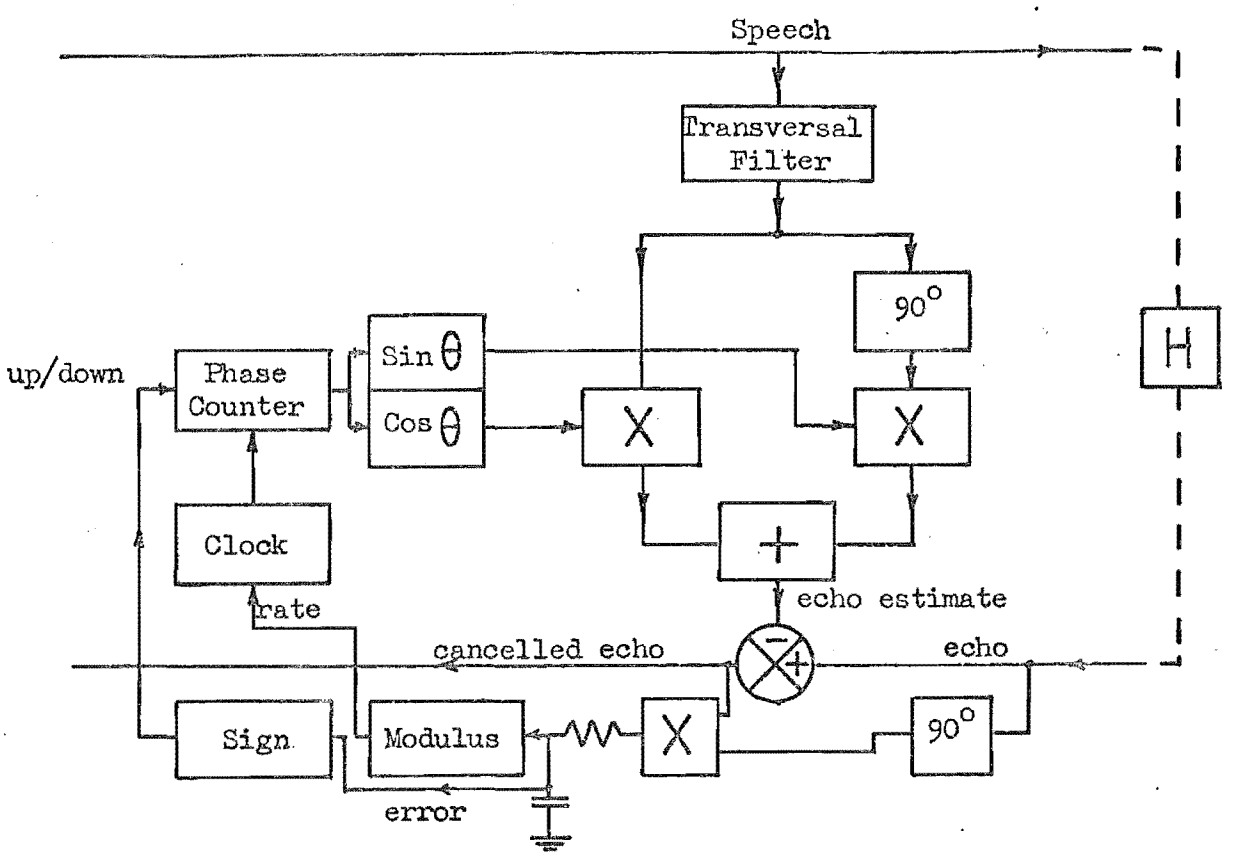


Fig. 5.6 A Complete Phase Tracking Structure

5.3.3 Estimating Phase Roll

As phase roll is constant due to the stability of oscillators in a frequency division multiplexed system an estimate of the frequency shift or rate of change of phase around the echo path would be valuable a priori information for a phase tracking system.

If identical PRN sequences are transmitted in succession the response to each will be identical if no phase roll is present. If the response is converted to a vectorial representation in polar form the phase shift between successive sequences can be measured and averaged. To be compatible with the single sequence testing proposed, the 1023 length sequence would be replaced by two 511 length sequences as illustrated in Fig. 5.7.

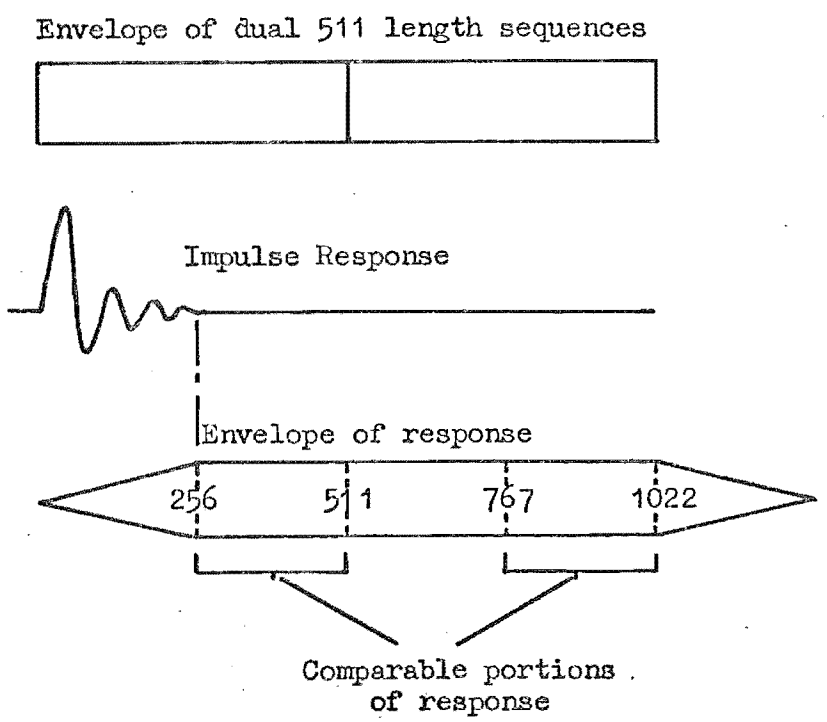


Fig. 5.7 Dual Sequences for Measuring Phase Roll

As the active period of the impulse response is known to occur within a 256 sample period the response to the sequence will have reached a steady state after this period, and will remain in a steady state until the end of the transmitted sequence. As the total response is 1022 + 256 samples long the samples of the response from 257 to 1022 are in this steady state. As the two consecutive sequences are the same, the sampled response between 256 to 511 and 767 to 1022 will be the same in the absence of any time variance. If, however, phase roll is present the magnitude of the vector will remain the same but the phase will change. By generating the quadrature component of the response samples the phase variation between these two sets of samples can be calculated. Averaged over the 256 sets of pairs this would give an accurate measurement of the phase roll. As phase roll is known to be less than 5 Hz there is no phase ambiguity for samples spaced by 511 samples or 64 mS. A diagram showing the possible structure of such a phase roll measurement system is found in Fig. 5.8.

This phase shift would destroy the validity of calculating the filter coefficients by a direct correlation of the response with the transmitted sequence. Once the phase roll is calculated, however, the response can be corrected to give the response for zero phase roll, and the appropriate filter coefficients can be calculated.

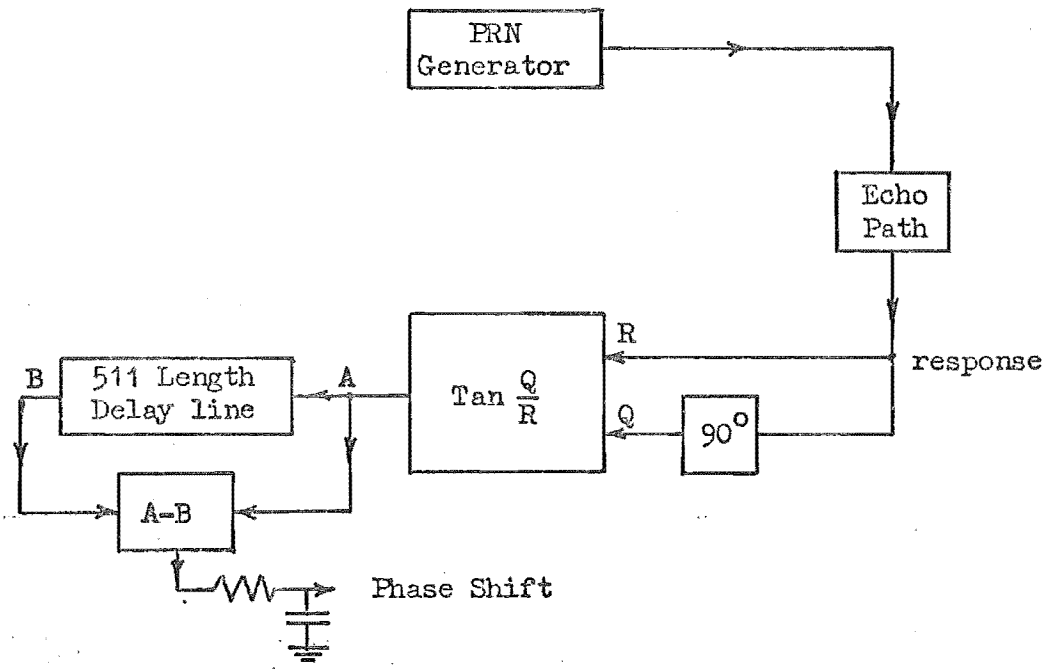


Fig. 5.8 Practical Measurement of Phase Roll

CHAPTER SIX

THE HILBERT TRANSFORM AND ITS APPLICATION TO PHASE ROLL

6.1 INTRODUCTION

The Hilbert Transform is a mathematical relationship between the real and quadrature components of real signals. By realising the Hilbert Transform in the time domain as a transversal filter the quadrature component of a signal with a wide bandwidth can be generated. This method of generating a 90° phase shift has wider application and is a technique using modern technology to solve a problem which has always been difficult. The most common application for a quadrature component is in the generation of an S.S.B. signal by the phasing method.

There are limitations in this method of generating a quadrature component. The necessity to limit the impulse response of the filter to a finite length and the finite sampling period associated with a transversal filter provide some restrictions. With suitable choice of a window function to truncate the infinite impulse response, and careful choice of sample period this method can be very satisfactory.

6.2 THE CONTINUOUS HILBERT TRANSFORM

By definition two signals are in quadrature if they are related by the Hilbert Transform pair;

$$s^*(t) = \frac{1}{\Pi} \int_{-\infty}^{+\infty} \frac{s(\tau)}{t-\tau} \, d\tau \tag{6.1}$$

$$s(t) = -\frac{1}{\Pi} \int_{-\infty}^{\infty} \frac{s^*(\tau)}{t-\tau} \, d\tau \tag{6.2}$$

The term quadrature relates to the effect of what is actually a convolution integral when it is transformed to the frequency domain through the fourier transform. All positive frequencies are phase shifted by $-\Pi/2$ and all negative frequencies by $+\Pi/2$, the spectrum of the effective transfer function being $-j \, \mathrm{sgn}(\omega)$ where $j = (-1)^{\frac{1}{2}}$ and $\omega = 2\Pi f$.

The impulse response of a network that will achieve this operation is given by the response of the network to a dirac delta function;

$$\delta^*(t) = \frac{1}{\Pi} \int_{-\infty}^{\infty} \frac{\delta(t)}{t-\tau} \, d\tau \tag{6.3}$$

$$= \frac{1}{\Pi t}$$

or the inverse fourier transform of the frequency spectrum;

$$\delta^*(t) = \frac{1}{2\Pi} \int_{-\infty}^{\infty} -j \, \mathrm{sgn}(\omega) e^{j\omega t} \, d\omega \tag{6.4}$$

$$= \frac{1}{\Pi t}$$

As the impulse response is not complex it can be realised by a circuit except for the complication of the impulse response extending into negative time and being infinitely long. The complication of negative time can be overcome satisfactorily by generating a component which is in quadrature with a delayed version of the real component. To overcome the problem of infinite length, the impulse response can be suitably truncated to a practical length. These considerations are best understood by developing the Discrete Hilbert Transform as a special case.

6.3 THE DISCRETE HILBERT TRANSFORM

A filter or network with such a transfer function can be approximated by realising the convolution equation (6.1) using a tapped analogue delay line. The extent to which the finite sample period and overall length affect the accuracy of this approximation are studied.

6.3.1 Sample Period Limitation

If the input signal is sampled and fed into a tapped delay line at equally spaced discrete points in time, the normal limitations apply for the sampling of any function. If the sampling rate is f_s the continuous case is approached as f_s approaches infinity. The taps are weighted inversely proportional to their distance from the centre of the line both in sign and magnitude. This corresponds to the centre representing time $t = 0$ with the tap weights corresponding to the samples of the impulse response $1/(\Pi t)$. The diagram in Fig. 6.1 illustrates this arrangement.

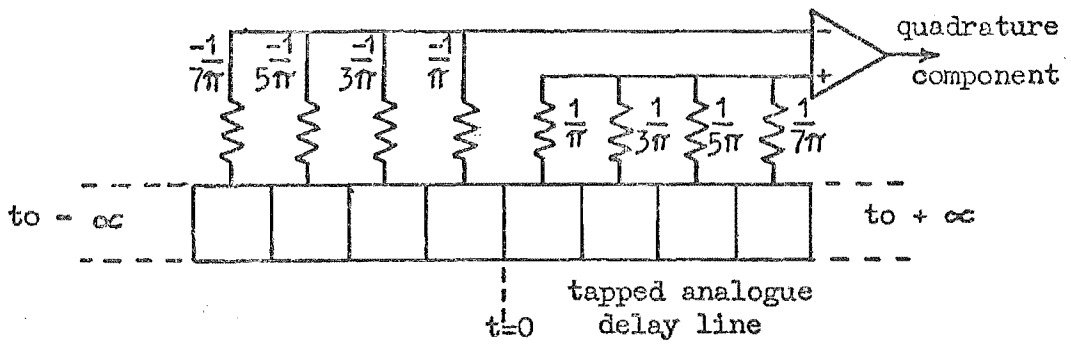


Fig. 6.1 Hilbert Transform Weighting of a Tapped Delay Line

In the limiting case as the length approaches infinity and the tap spacing zero this circuit approaches the continuous convolution equation;

$$s^*(t) = \int_{-\infty}^{\infty} h(\tau)s(t-\tau)\,d\tau \qquad (6.5)$$

where $s(t)$ is the input signal

and $h(t)$ the impulse response $1/(\Pi t)$

or in the discrete case;

$$s^*(kT) = \sum_{i=-\infty}^{+\infty} h(iT)s((k-i)T) \qquad (6.6)$$

If the sampling rate is f_s then the time delay between taps is $\tau_s = 1/f_s$ and the range of frequencies to which the input must be limited to obey the sampling theorem is 0 to $f_s/2$. Assuming initially an infinite length delay line the response of the line to a band-limited impulse is;

$$s^*(t) = \frac{1}{2\Pi j}\int_{-\omega_o}^{\omega_o} \text{sgn}(\omega)\, e^{j\omega t}\, d\omega \tag{6.7}$$

$$\text{where } \omega_o = 2\Pi f_s/2$$
$$= \Pi/\tau_s$$

therefore;

$$s^*(t) = \frac{1}{\Pi t}\,(1 - \text{Cos}\ \omega_o t) \tag{6.8}$$

$$= \frac{1}{\Pi t}\,(1 - \text{Cos}\ \frac{\Pi t}{\tau_s}) \tag{6.9}$$

The second part of the Hilbert pair is the real part band-limited to ω_o;

$$s(t) = \frac{1}{2\Pi}\int_{-\omega_o}^{\omega_o} e^{j\omega t}\, d\omega \tag{6.10}$$

$$= \frac{\text{Sin}\ \omega_o t}{\Pi t} \tag{6.11}$$

$$= \frac{1}{\Pi t}\ \text{Sin}\ \frac{\Pi t}{\tau_s} \tag{6.12}$$

A diagram showing the impulse responses for the real and quadrature components for the band-limited case governed by the sampling rate f_s is given in Fig. 6.2.

Fig. 6.2 shows that if the sampled signal is fed into a lumped delay line then the sum of every second tap in accordance with the impulse response $s^*(t)$ will generate a quadrature component relative to the real signal s(t) being extracted from the centre tap of the line. The band-limited

response s(t) being the impulse response for the real component delayed in time by half the length of the line. It also shows that the delay line needs only be tapped or sampled at intervals of 2 or half the nyquist rate to get a bandwidth of $f_s/2$. The bandwidth of the Hilbert Transform appears to reach out to the sampling frequency, having double the normally accepted bandwidth. This does not mean, however, that the signal can be sampled at half the nyquist rate as samples must still be generated at the nyquist rate.

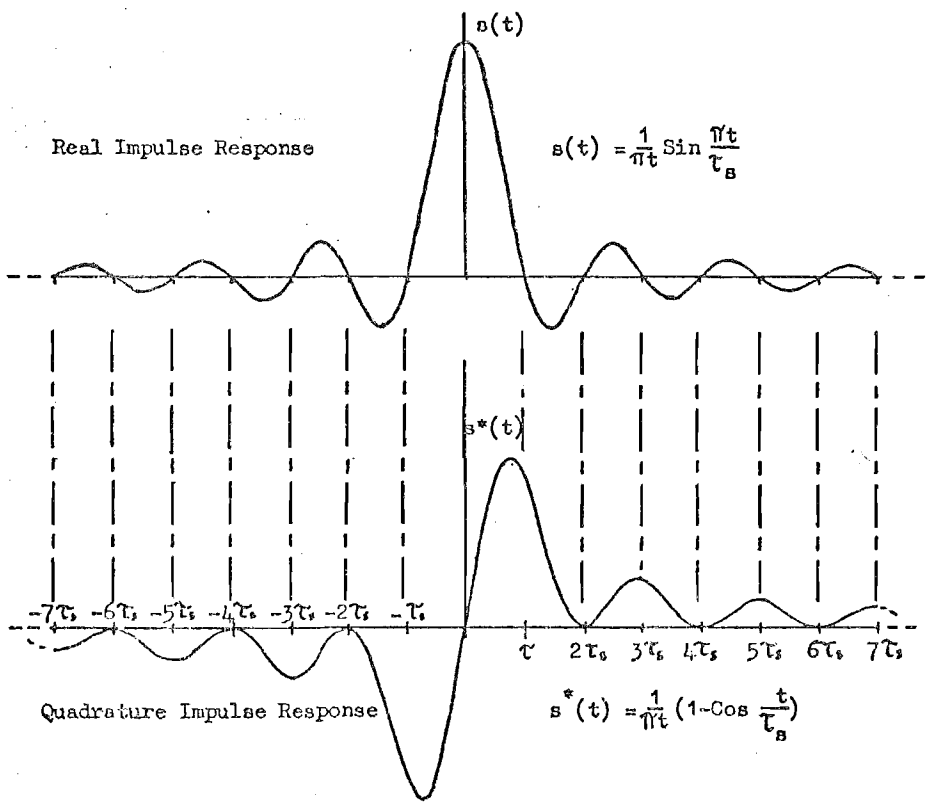


Fig. 6.2 Band-limited Hilbert Pair

6.3.2 Finite Length Limitation

If the length of the line is simply truncated at +/- (T/2) the fourier transform of the truncated impulse

response becomes;

$$\delta^{*}(\omega,T) = \frac{1}{\Pi}\int_{-T/2}^{+T/2}\frac{e^{-j\omega t}}{t}\,dt \qquad (6.13)$$

$$= \frac{2}{j\Pi}\,\frac{\mathrm{Sin}(\omega T/2)}{(\omega T/2)} \qquad (6.14)$$

which remains true quadrature but the amplitude of the spectral components are modified significantly if the length is short. This is the problem which is encountered in many signal processing applications and is termed 'windowing'. In the above example the window is the basic rectangular window which is of length T and of unity height. The continuous function is multiplied by the window in the time domain and the effect on the amplitude spectrum is the convolution of the fourier transforms of both functions.

6.3.3 Improvements with Windowing

Windows are used in digital signal processing primarily to smooth out discontinuities in the time domain which when transformed into the frequency domain or fourier domain, modify the transform of the original function. This is particularly apparent where the discrete fourier transform (or FTT) is being used to transform non-periodic waveforms or data. The inherent assumption in discrete time processing is that the waveform or data being processed is periodic. Any non-periodic function that is to be used must, therefore, be modified or truncated and assumed to be periodic over

that length. If this function is not repetitive over this period, the simple truncation in the form of the previously mentioned rectangular window will result in a discontinuity in the function as it is assumed to be periodic.

If the function being processed is periodic, then the fourier transform will have discrete components at multiples of the fundamental frequency. The application of a rectangular window on such data has no affect as the spectrum of the window has zero's at all harmonics of the fundamental including the fundamental. It is only in the case of non-periodic functions that other than rectangular windows must be applied.

The fourier transform of the window function itself provides the information to determine the effects on the correct spectrum. As already mentioned the resultant spectrum is the convolution in the fourier domain of the transforms of the two individual functions. The windowing of the impulse response for the Hilbert Transform provides a good illustration of the effects of windowing. The functions shown in Fig. 6.3 illustrate the effect of simply truncating the otherwise infinitely long impulse response. It is not difficult to see that the resulting spectrum is in fact the convolution of the individual spectrums. As the length of the window approaches infinity the spectrum will approach the periodic rectangular waveform, with the spectral component spacing decreasing to zero. As the sample

spacing of the window decreases to zero the period of the rectangular spectrum increases to infinity as in the continuous case.

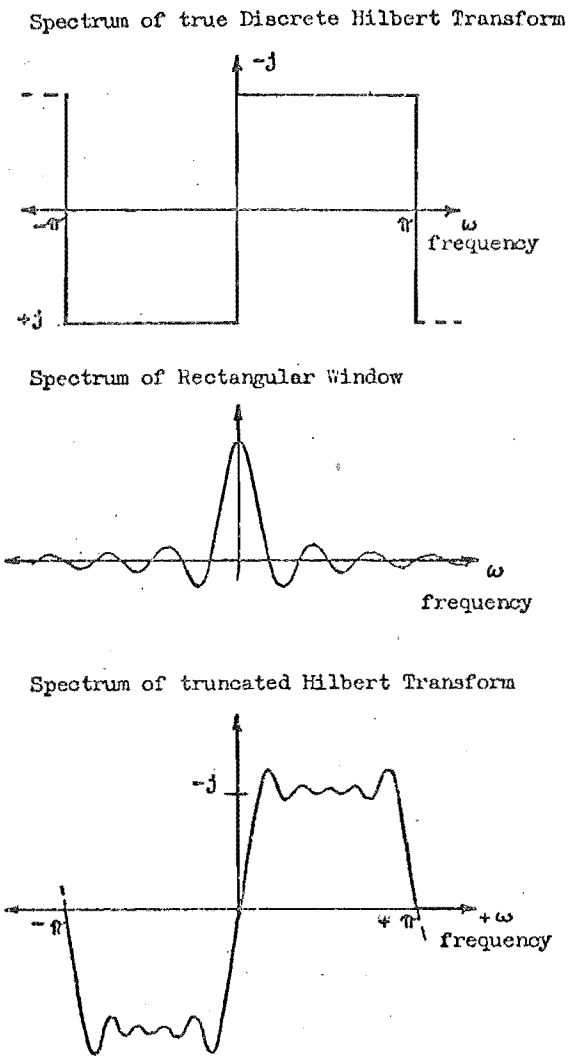


Fig. 6.3 Spectrum of the Hilbert Transform when Truncated using a Rectangular Window

Some guidelines for the choice of a suitable window can be drawn from the above diagram. There are two main properties of the fourier transform on the window and in general any choice made is a trade-off between these

properties. The main properties are the width of the main lobe and the amplitude of the sidelobes.

The ideal window of course is infinitely long and of equal height so no truncation of the function occurs. The transform of this is a dirac delta function which has infinitely narrow main lobe and zero side lobes. When this is convolved with the transform of the function concerned no change results. This is the case of the continuous fourier transform. It is, therefore, desirable to approximate this result as closely as possible with a finite length window, by having a window with a very narrow main lobe with minimal side lobes.

The width of the main lobe contributes directly to the bandwidth of the resultant spectrum. The wider the main lobe the less steep are the skirts of the resultant function in the fourier domain. The discrete Hilbert Transform ideally has vertical skirts and, therefore, illustrates this property clearly. The amplitude of the side lobes determines the amount of ripple on the function. In the case of the rectangular window the first few side lobes are large in amplitude causing the ringing effect on the resultant spectrum. The choice of window is, therefore, made with these properties in mind. The pattern on the sidelobes varies considerably with some decaying rapidly, others having many side lobes and in the case of the Dolph-Chebyshev Window, continuous side lobes all of equal amplitude.

A good summary of windows and their properties is given by Harris[48] which provides a basis for choosing a suitable window. Some of the more common windows are illustrated in Fig. 6.4.

6.3.4 The Dolph-Chebyshev Window

This window is particularly suited to discrete time signal processing and gives the narrowest main lobe for any given level of side lobes. It equalises all levels of side lobes to a given permissible maximum to achieve a very narrow main lobe. This is achieved by specifying the fourier transform of the window using the conventional Chebyshev polynomial and using the FTT to do an inverse fourier transform to obtain the window 'weights'.

This window is of only limited use in the continuous case, such as shading of antennas due to impulses or discontinuities at the boundaries. No such limitation exists, however, for the discrete case.

The Chebyshev polynomial

$$\frac{\mathrm{Cos}\{\ N\ \beta \mathrm{Cos}^{-1}(\beta\ \mathrm{Cos}\pi k/N)\}}{\mathrm{Cosh}(\ N\ \mathrm{Cosh}^{-1}(\beta))}$$

describes the discrete fourier domain representation where;

$$-\tfrac{1}{2} \leq k/N < +\tfrac{1}{2}$$

and

$$\beta = \mathrm{Cos}\{(1/N)\ \mathrm{Cosh}^{-1}(10^{\alpha})\}$$

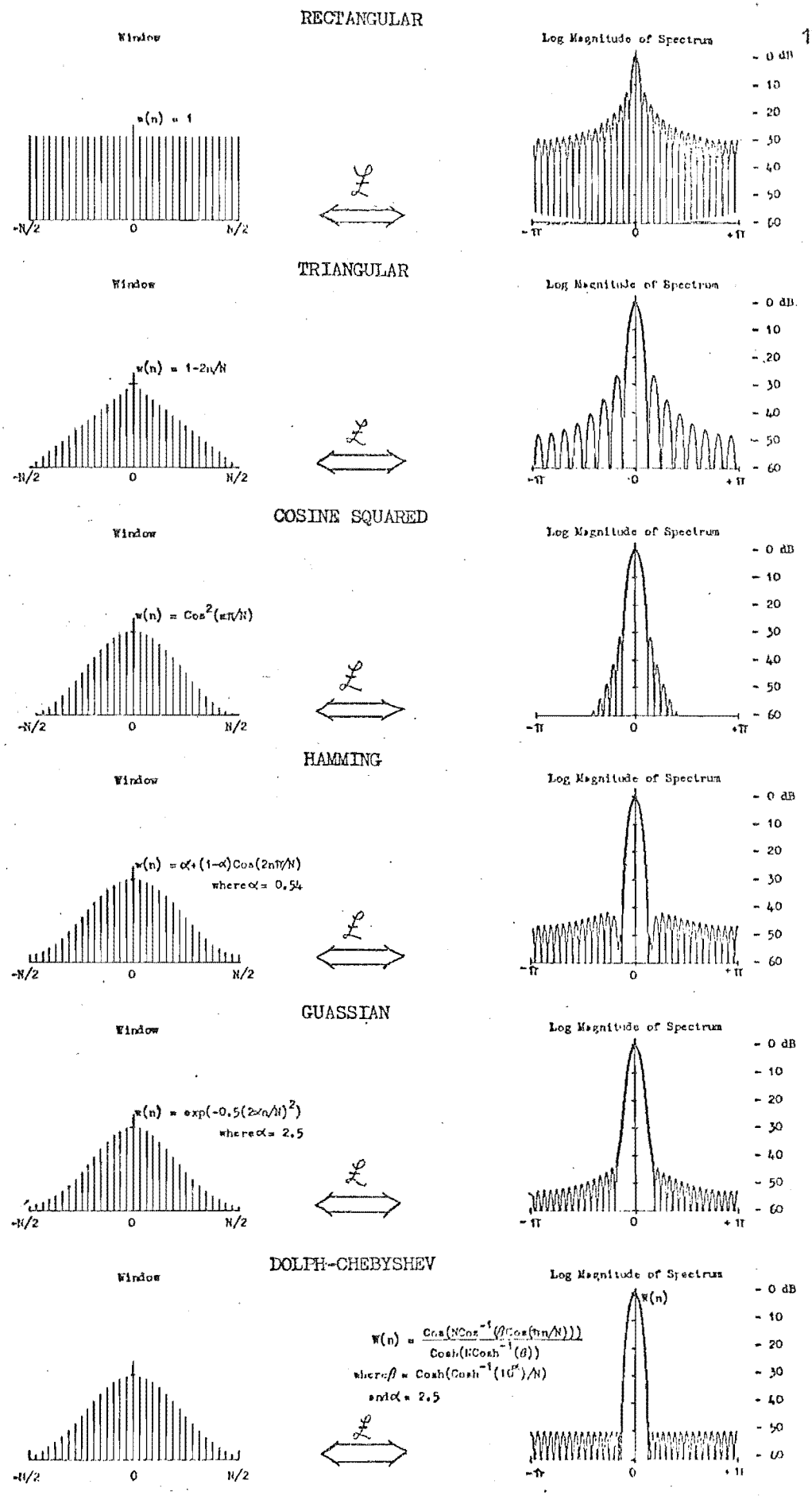


Fig. 6.4 Some Common Windows and their Fourier Transforms

where α is the relative level of the main lobe to side lobes in decades. e.g. if $\alpha = 3$ the main lobe level is 60 dB above the sidelobes. This parameter is, therefore, a variable which can be chosen to set the side lobes at a maximum permissible level, to obtain the narrowest possible main lobe for that amount of ripple. A diagram showing the equi-ripple spectrum of the window is shown in Fig. 6.5. A further diagram showing its effect on the spectrum of the Hilbert Transform can be seen in Fig. 6.6.

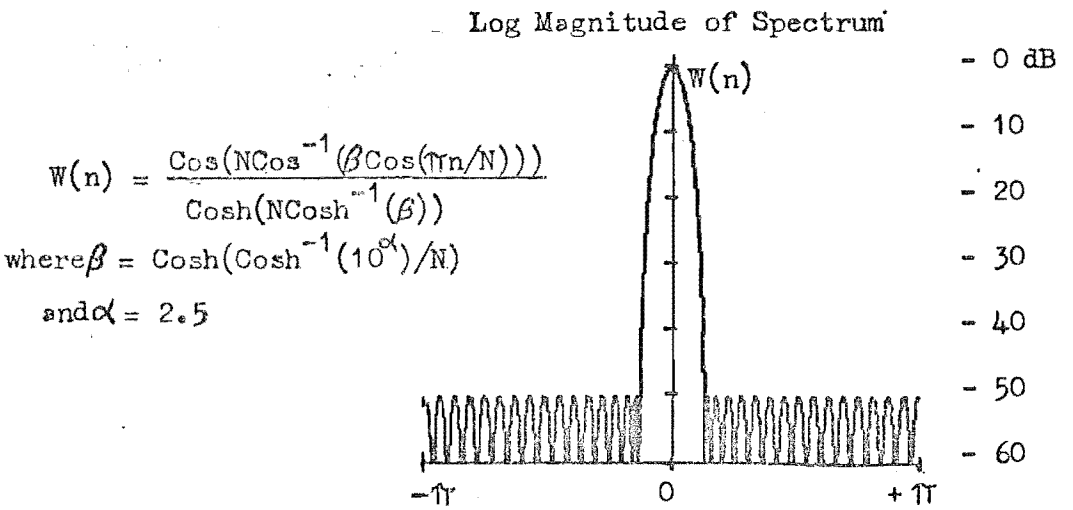


Fig. 6.5 Equi-ripple Spectrum of Dolph-Chebyshev Window

$$W(k) = \frac{(-1)^k \mathrm{Cos}\{N\ \mathrm{Cos}^{-1}(\beta \mathrm{Cos}(\Pi k/N))\}}{\mathrm{Cosh}(N\ \mathrm{Cosh}^{-1}(\beta))}$$

for $-\frac{1}{2} \leqslant k < \frac{1}{2}$

where $\mathrm{Cos}\{N\ \mathrm{Cos}^{-1}(X)\} = \mathrm{Cosh}\{N\ \mathrm{Cosh}^{-1}(X)\}$ for $|X| \geqslant 1$

and $\mathrm{Cos}^{-1}(X) = \Pi/2 - \mathrm{Tan}^{-1}\{X/(1-X^2)^{\frac{1}{2}}\}$

and $\mathrm{Cosh}^{-1}(X) = \ln\{X+(X^2-1)^{\frac{1}{2}}\}$

The term $(-1)^k$ ensures that the output from the FFT is in a suitable form and the removal of it only results in a time shift.

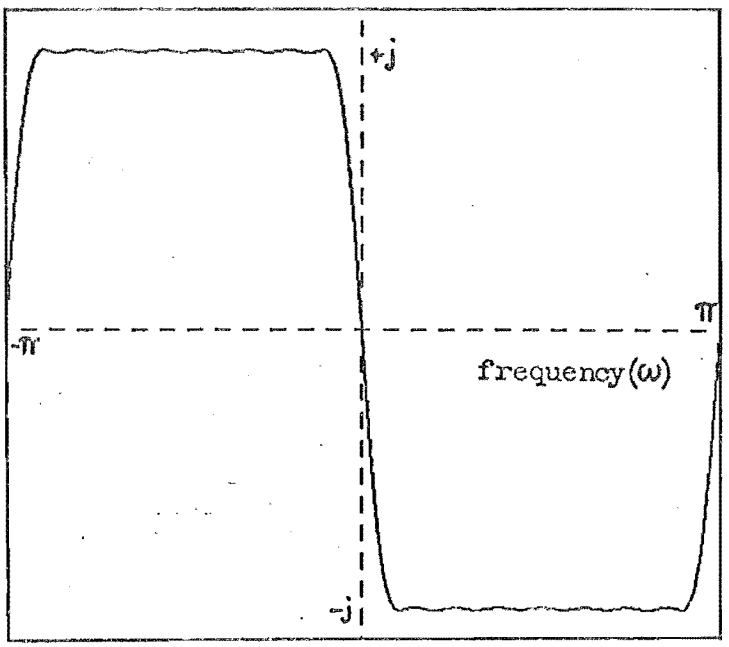


Fig. 6.6 Amplitude Spectrum of Dolph-Chebyshev Windowed Hilbert Transform

6.4 REAL TIME GENERATION OF THE HILBERT TRANSFORM PAIR

The windowed discrete time domain representation of the Hilbert Transform h(kT) can be used as filter coefficients for a transversal filter to generate two quadrature components of a sampled signal s(kT). By convolving s(kT) with the impulse response h(kT) using an analogue tapped delay line two components in quadrature can be generated. The appropriate equation being;

$$s_q(kT) = \sum_{i=-\infty}^{\infty} h(iT)\, s_r\{(k-i)T\}$$

where $s_r(kT)$ is the real component being a delayed version of $s(kT)$, $s_q(kT)$ is the quadrature component and $h(kT)$ is discrete impulse response of the windowed Hilbert Transform.

The real component $s_r(kT)$ appears at the centre of the tapped delay line as illustrated in Fig. 6.7. The quadrature component is the sum of the odd numbered taps as numbered from the centre of the line - the centre being tap 0 - with the tap weight being inversely proportional to the distance from the centre of the line multiplied by the window weight.

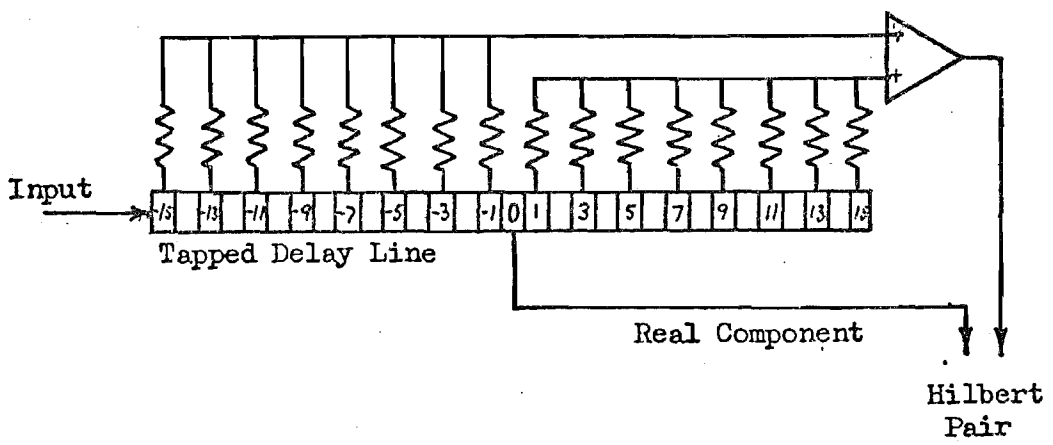


Fig. 6.7: Real Time generation of Hilbert Pair

The limitation of the delay on the real component can be accommodated in echo canceller design. The delay associated with a 32 tap delay line will be 8 sample periods or 2 mS. This can be accommodated either within the initial delay period of the impulse response prior to the activity, or by inserting extra delay with a fixed delay line in the echo path. The spectrum of the Hilbert Transform using a 32 tap delay line, with the window chosen for $\alpha = 2.5$ was shown in Fig. 6.6. This gives more than sufficient bandwidth and amplitude accuracy to generate any phase shift to compensate for phase roll. The method by which any phase shift is generated and the subsequent application to generating a frequency shift or phase roll has been covered in Chapter 5.

CHAPTER SEVEN

NON-ADAPTIVE, LOGARITHMIC, MULTIPLEXED ECHO CANCELLER

7.1 INTRODUCTION

All aspects of echo canceller design have been considered and an echo canceller has been developed which is less complex than other comparable designs. With the possibility of providing phase tracking facilities independent of the basic canceller circuitry, this design could have wider application. The less complex nature of this canceller and the multiplexing of expensive components makes it economically and technically attractive.

The canceller has three characteristic features. It is non-adaptive in that it does not continually adjust to circuit variations but uses fixed filter coefficients obtained from the response to an interrogation signal. It uses a true logarithmic format for storing and processing speech samples and filter coefficients, to reduce storage and more importantly to simplify the convolution process. Finally the expensive components used for analogue to digital, linear to logarithmic and digital to analogue conversion along with the circuitry for calculating filter coefficients are multiplexed over many channels. This

reduces the amount of channel-dedicated components to a minimum and reduces the per channel cost significantly.

Rather than design an individual canceller it was necessary or at least preferable to consider the overall requirements in terms of the number of circuits both at present and in the future. The existing number of New Zealand international circuits was 50 with a predicted 150 being required in the foreseeable future. The structure of the telephone network is such that all the international circuits out of New Zealand pass through the gateway exchange at Auckland. This enables the physical grouping of channel dedicated equipment and permits multiplexing of components where desired.

It was, therefore, decided to base the design around an eventual target of 150 channels but to provide for gradual addition of required channel-dedicated equipment as channels increased. Certain sections of the canceller would necessarily be channel-dedicated and obviously one complete set of this equipment would be required per channel. The division of channels on multiplexed equipment would be determined by the usage rate per channel.

Although initially it was envisaged that a microprocessor based monitoring system would be used for many of the control tasks and system identification this was later considered impractical. The main limitation on such an application is the low speed of a microprocessor relative to what can be achieved with hard-wired circuitry.

7.2 MULTIPLEXED CIRCUITRY

It has been established that the canceller generates an estimate of the echo by realising the convolution equation;

$$e'(kT) = \sum_{i=0}^{255} h(iT)s\{(k-i)T\}$$

where $e'(kT)$ is an estimate of the real echo sample $e(kT)$,

$h(kT)$ is the model of the impulse response of the channel, established by the canceller,

and $s(kT)$ is the incoming speech to the canceller and national network.

By calculating $h(kT)$ and converting it along with the speech samples $s(kT)$ to log format the convolution equation becomes;

$$e'(kT) = \sum_{i=0}^{255} \text{antilog}\{\log(h(iT)\} + \log\{((k-i)T))\}$$

Apart from the processing shown by the equation A/D and D/A conversions and the calculation of $h(kT)$ are required;

$s(t)$	$\rightarrow$	$s(kT)$	analogue to digital
$e'(kT)$	$\rightarrow$	$e'(t)$	digital to analogue

The measurement and calculation of the filter coefficients or impulse response samples will be detailed in Section 7.3.

To determine what sections of the canceller are suited to multiplexing it is necessary to study a diagram of the

complete canceller, except for that associated with impulse response measurement. This block diagram is shown in Fig. 7.1.

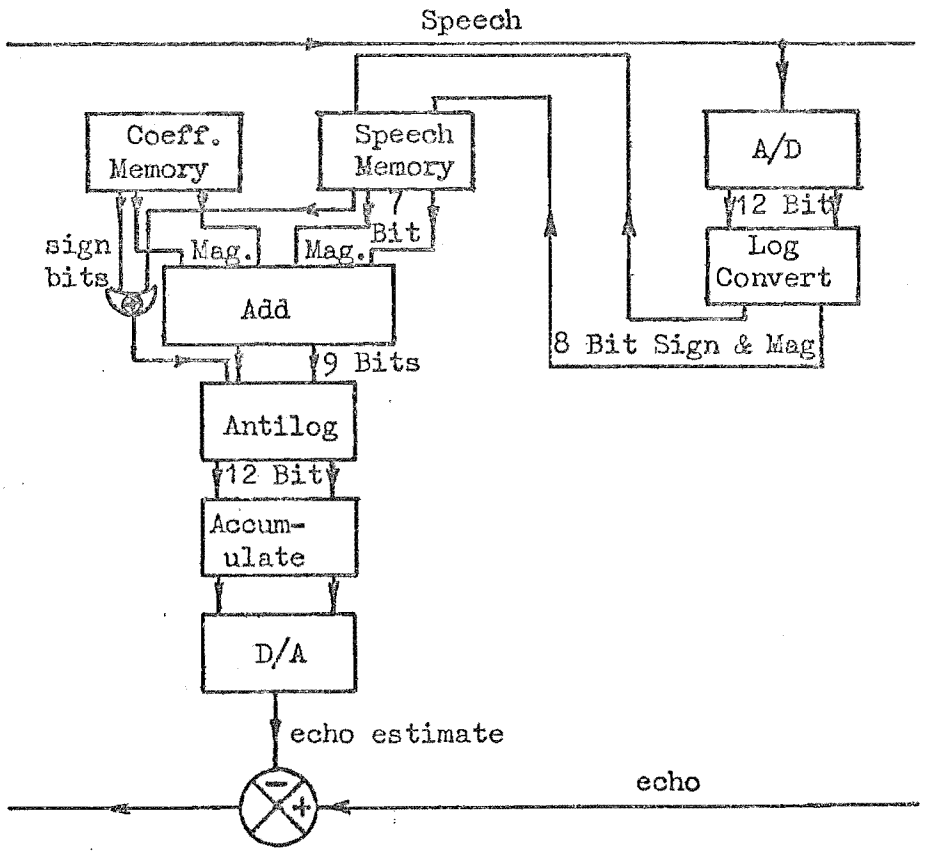


Fig. 7.1 Overall Echo Canceller Circuitry

To contemplate the advantages of multiplexing any or all of the above components it is necessary to consider the duty cycle of each if allotted to one canceller only. From this the maximum number of channels it could serve is known. A further consideration is the convenience, practicability and cost advantage of time sharing at each stage.

7.2.1 Analogue to Digital Conversion

This process involves the periodic sampling of a continuous analogue waveform s(t) - in this case at an 8 KHz rate. This sampled amplitude is held until the analogue to digital conversion is completed. This process is illustrated in Fig. 7.2.

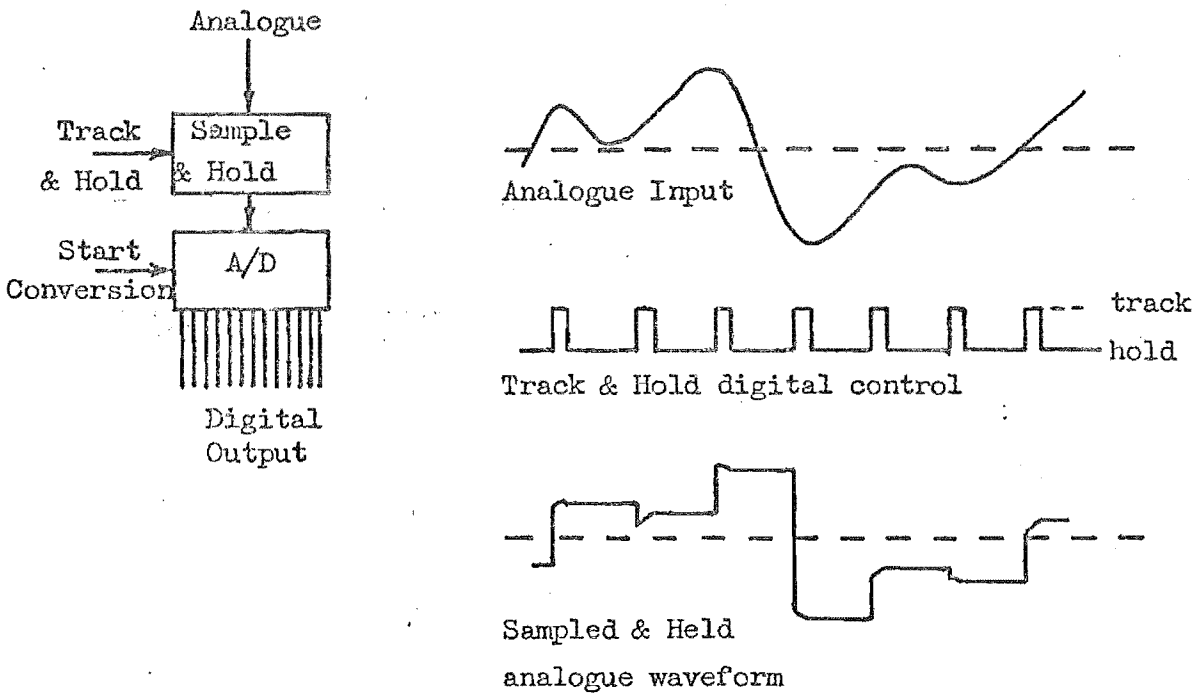


Fig. 7.2 Analogue to Digital Conversion and Sample and Hold Waveforms

The combined time required for these two operations depends on the particular components used. Sample and hold amplifiers suitable for 12 bit accuracy range in cost from $300 to $20 depending on speed. 12 bit A/D convertors with adequate conversion times vary in price from $300 to $100. As the minimum combined time of these conversions is around

3 uS and the operation occurs only once every 125 uS (8 KHz sampling rate) and the combined cost of $600 can be shared over as many as 40 channels. When a further 1 uS is allowed for time multiplexing this reduces to 30 channels giving a per channel cost of $20 compared with $100 if slower, cheaper channel dedicated components were to be used. This means that five groups of A/D conversion circuits are required for 150 channels. A suitable arrangement is shown in Fig. 7.3.

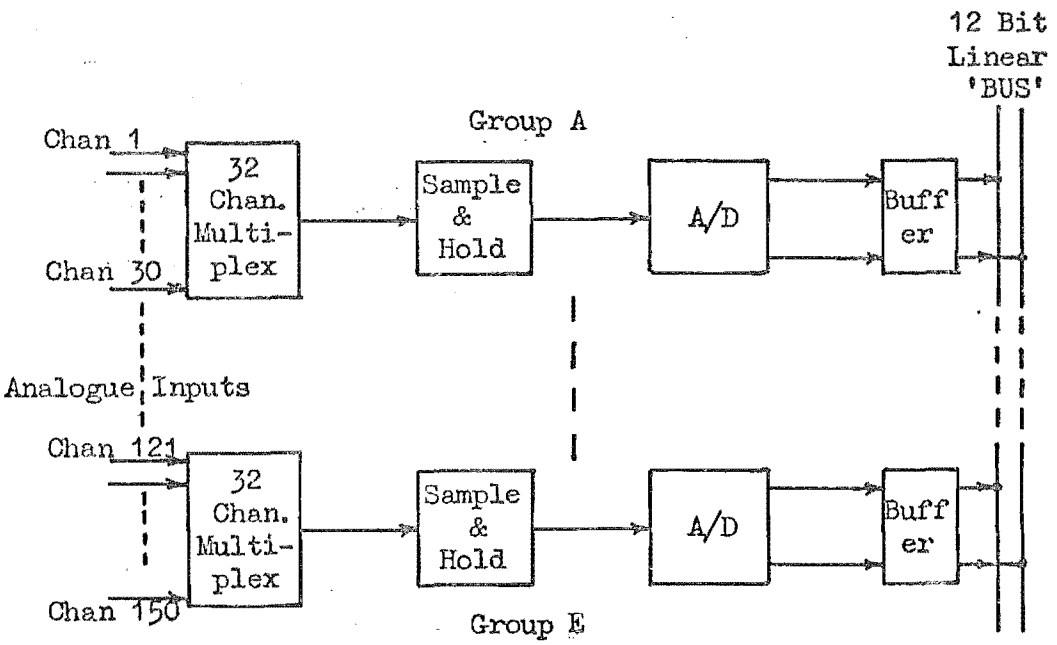


Fig. 7.3 Multiplexing of Analogue to Digital Conversion Circuitry

The digital linear signal sample appears on the 12 bit linear 'BUS' at a different time for each channel with control circuitry synchronising the individual channel timing to the multiplexer.

7.2.2 Linear to Logarithmic Conversion

This circuitry is an obvious candidate for multiplexing. It consists of a Programmable Read Only Memory (PROM) programmed as a logarithmic look-up table. It converts an 11 bit linear magnitude forming the address, to a 7 bit logarithmic magnitude at the output. A simple explanatory diagram of this process is shown in Fig. 7.4.

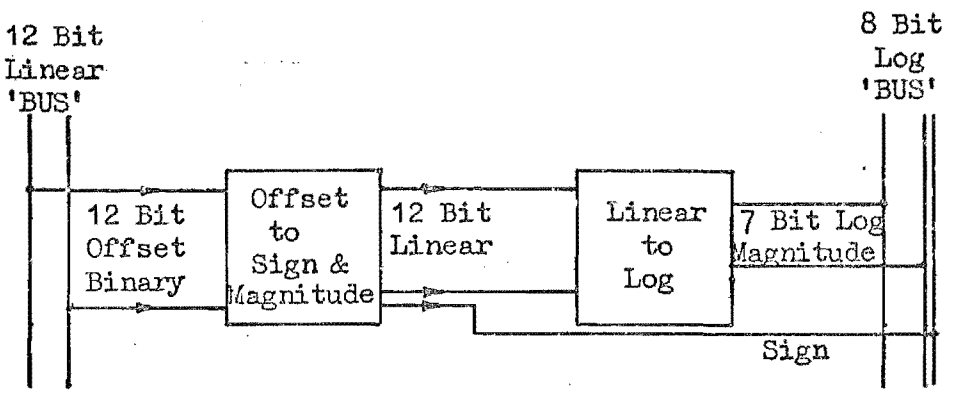


Fig. 7.4 Linear to Logarithmic Conversion Multiplexing

Fusible link PROMs have typical access time of around 50 nS meaning that one could be shared over a maximum of 250 channels and, therefore, could provide conversion for all channels in the multiplexed system. The PROM is a 2048 x 8 representing 16K of memory, however, only 7 of the output bits are used. The cost of this on a per channel basis is negligible. The output of this memory is available to the

input of all channels and each channel accepts its appropriate sample at the correct time. The input originates from the output of the 5 A/D convertor circuits which would be multiplexed onto the linear 'BUS' providing the input to this convertor.

7.2.3 Digital to Analogue Conversion

The multiplexing of D/A convertors is also economical and convenient. These convertors cost around $60 for 12 bit applications virtually irrespective of speed. It is, therefore, advisable to cost share this over 30 channels as in the case of the A/D convertors. With a conversion speed of 1 uS it could be used for more channels but to give some degree of standardisation in the A/D and D/A interfacing 30 channels

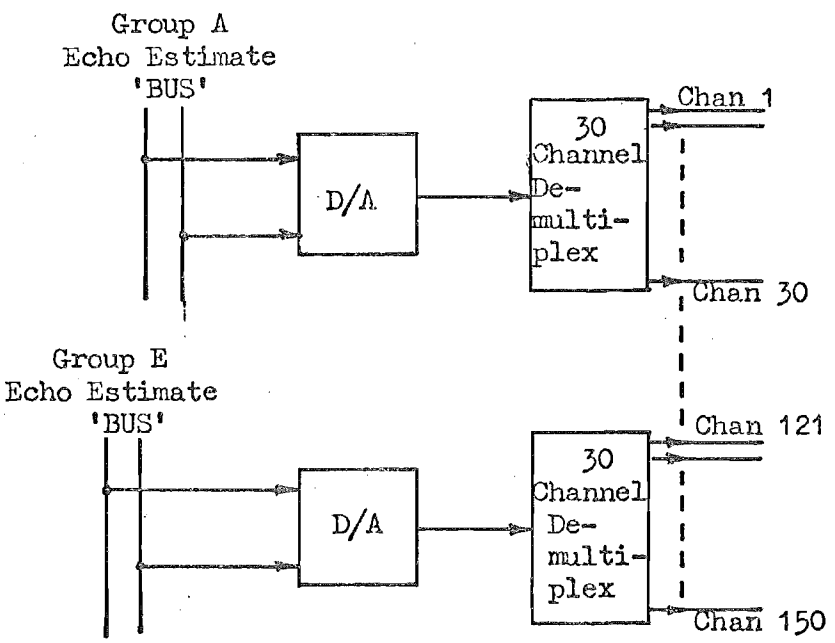


Fig. 7.5 Digital to Analogue Multiplexed Conversion

was considered appropriate. The 30 channels associated with each convertor are connected to the group 'BUS' forming the input to the convertor with the output being switched with an analogue de - multiplex switch to the analogue boards of these 30 channels. This D/A convertor multiplexing is illustrated in Fig. 7.5.

7.3 CALIBRATION CIRCUITRY

The aim of this circuitry is to calculate the coefficients for the digital transversal filter which models the filter path. This is achieved by transmitting a 1023 length pseudo random sequence, measuring and storing the response of the echo path and calculating from this response the filter coefficients. This process can be divided into two distinct cycles; a transmit and measure cycle and a correlation cycle. As already established in Chapter 3, the coefficients are the result of correlating the response to the transmitted sequence with an extended version of the sequence.

The transmit and measure cycle takes 160 mS, the first 128 mS being the time the sequence is being transmitted. The response is being measured for the full 160 mS. The samples of the response are taken from the 12 bit linear 'BUS', having been measured and converted by the multiplexed A/D convertor associated with the particular circuit under test. During this cycle of operation the return end of the echo path is connected to the analogue output on the channel interface board for A/D conversion.

The correlation cycle involves 256 shifts each with 1280 multiplications and summations to realise the discrete correlation

$$h(kT) = \sum_{i=-k}^{1279-k} s'(iT)\,r\{(k+i)T\} \qquad \text{for } 0 \leqslant k \leqslant 255$$

where $r(kT)$ is the response of the echo path to the transmitted sequence $s(kT)$,

$s'(kT)$ is the extended version of the transmitted sequence $s(kT)$,

and $h(kT)$ is the discrete impulse response of the echo path.

These functions in the correlation equation are illustrated in Fig. 7.6

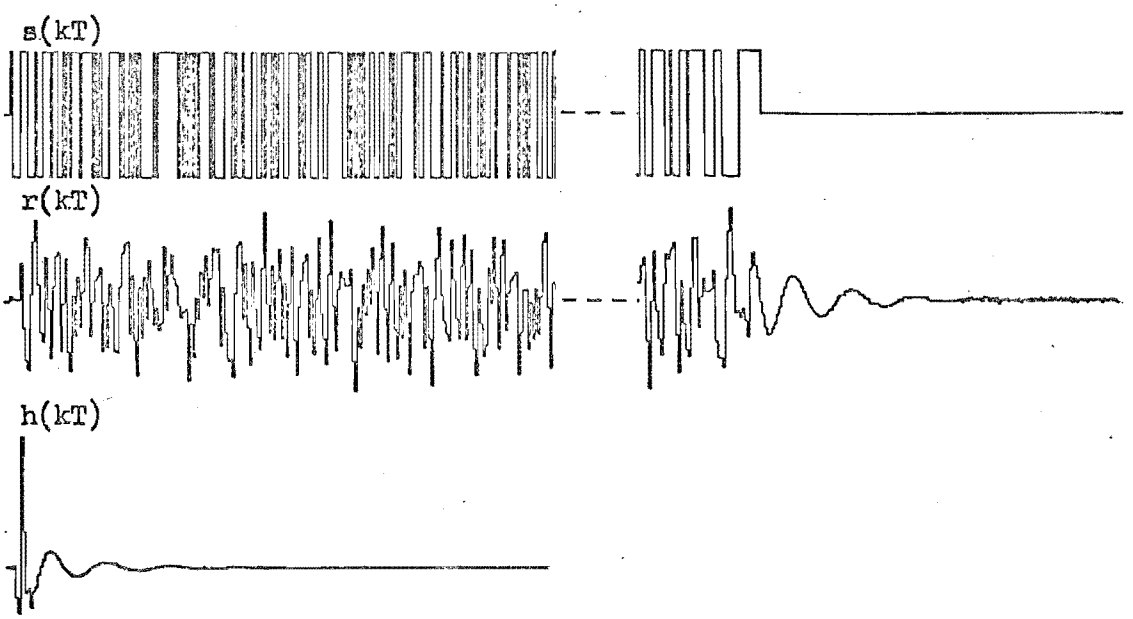


Fig. 7.6 Functions Involved in Correlation Process

As s'(kT) is a two level function (+/- 1) the products in the correlation are summations or subtractions only, depending on the sign of s'(kT). The time required for accessing memory to obtain r((k+i)T) is 450 nS for this particular static Random Access Memory, with a further 250 nS being required for the accumulation involving up to 10 bits of shift. The limit of 10 bits of shift or carry corresponds to the case where the impulse response is a delta function and r(kT) is identical to s(kT). A clock rate of 1.28 MHz is used for this correlation with each coefficient taking (1280 x 780)nS or 1 mS. All coefficients are, therefore, calculated in 256 mS following the 160 mS for the transmit and measure cycle. The total time required for calibration of one channel is, therefore, 416 mS.

With the expected rate of calibration at only twice per channel per 4 mins and the statistical distribution applying to circuit connections one calibration circuit is adequate to cover all channels. A block diagram showing the structure of this circuit is given in Fig. 7.7.

The output of the correlator applies the calculated filter coefficients back to the 12 bit linear 'BUS' during the time when signal samples form that channel would otherwise be present. The coefficients are then converted to logarithmic format in the same manner as signal samples. The correlator itself is shown in more detail in Fig. 7.8.

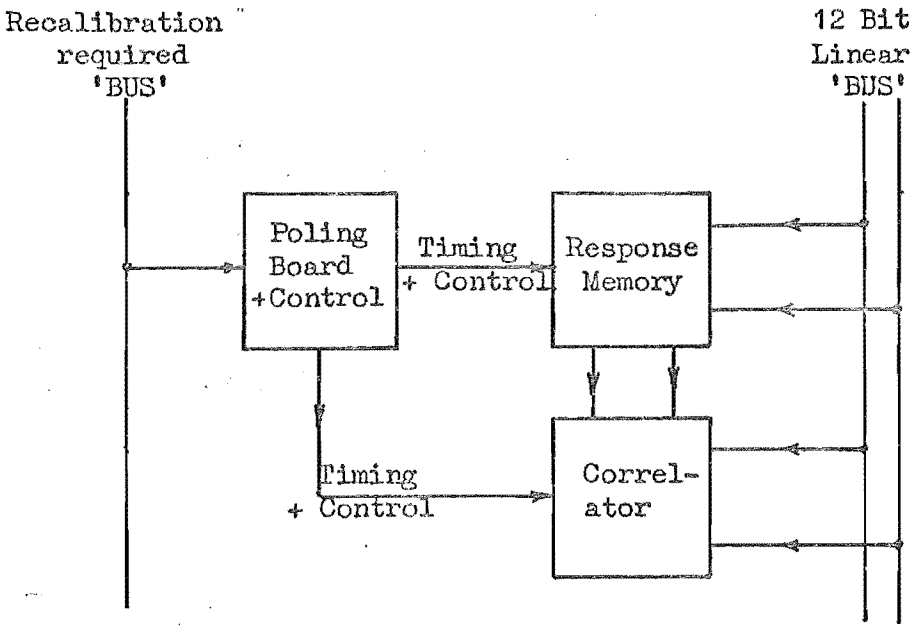


Fig. 7.7 Block Diagram of Calibration Circuitry

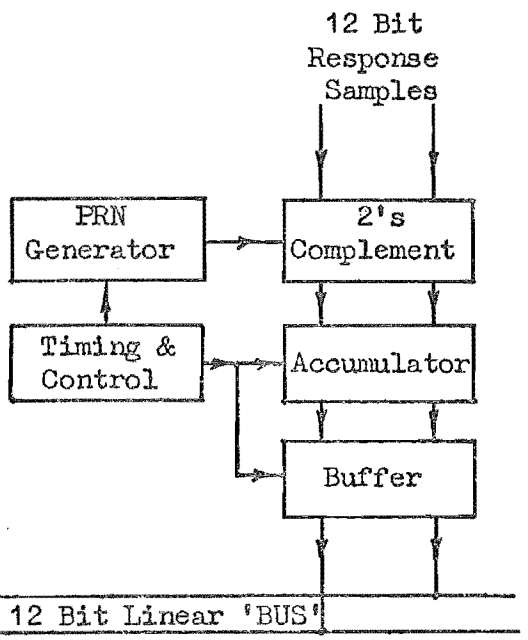


Fig. 7.8 Block Diagram of Correlator Circuitry

The poling board addresses all cancellers to search for a recalibration flag which is generated when the canceller is not operating satisfactorily. This flag appears on a common 'BUS' at a specific time for each channel. The channels are searched sequentially and as a channel needs recalibration the calibrator adopts the timing appropriate to that channel for purposes of synchronising to the correct data on any common 'BUS'.

7.4 CHANNEL ANALOGUE CIRCUITRY

This analogue circuitry is not suitable for multiplexing as the majority of it is an integral part of the 4 wire transmission circuit and, therefore, must be continuous. The main purpose of this circuitry is to provide a through path for incoming and outgoing speech while providing an output to the A/D multiplex circuitry at a suitable level. It also provides for the insertion of the transmitted sequence when the channel is under calibration. It is, therefore, an interface between the balanced 4 wire transmission circuit and the unbalanced analogue requirements of the canceller circuitry. It will be the only board required to remain 'in circuit' for otherwise normal circuit operation and, therefore, should have high reliability and minimum circuitry. Fig. 7.9 is a block diagram of this circuitry.

The incoming speech at 4W Rx In is amplified to the correct level for A/D conversion before passing through a summing circuit for the addition of noise when required. It is then low-pass filtered to limit the frequency range of the

noise. Then it is restored to the correct level before returning to the 4W Rx Out side of the transmission circuit.

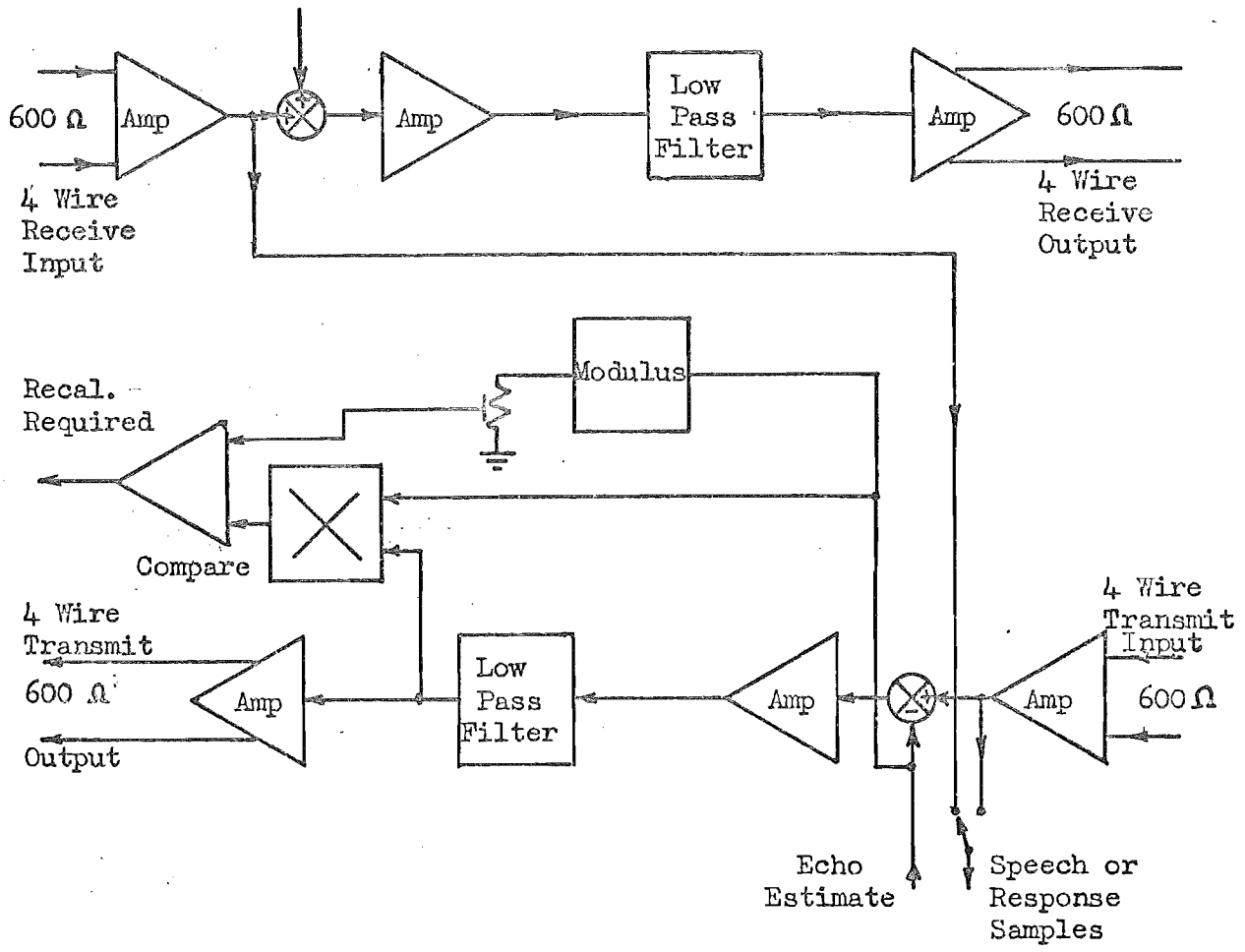


Fig. 7.8 Analogue Interface Circuitry

The return path at 4W Tx In is converted to an unbalanced circuit and adjusted in amplitude for the response of the noise sequence to be applied to the multiplex board at the correct level. The through signal is then subject to cancellation by the subtraction of the estimate generated by the convolution circuitry. The combined signal is low-pass filtered before being restored to the correct level and a balanced output. The echo estimate e'(kT) is held for only

about 10 uS instead of the full sample period to overcome the sin x/ x transfer function associated with a first order sample and hold circuit. This has the same effect as the modification to the transmitted noise sequence and will be understood by referring to Section 3.3.

The result of cancellation is multiplied by the echo estimate to give a measure of correlation between these points. If the estimate is correct it will have been cancelled and none of it will appear at this point and give zero correlation. This measure of the estimate appearing after this cancellation is compared with the amplitude of the estimate. If this reached a pre-determined proportion of the estimate the 'flag' indicating the need for recalibration is set. A mathematical treatment of this correlative check is shown in Appendix VI.

7.5 CONVOLUTION CIRCUITRY

The convolution board forms the basis of the digital transversal filter which generates the estimate of the echo by realisng the discrete convolution equation;

$$e'(kT) = \sum_{i=-\infty}^{\infty} h(iT)s\{(k-i)T\}$$

where $h(kT)$ is the discrete impulse response of the transversal filter,

$s(kT)$ is the incoming sample train,

and $e'(kT)$ is the resultant echo estimate.

As h(kT) is non-zero only for $0 \leqslant k \leqslant 255$ the equation becomes;

$$e'(kT) = \sum_{i=0}^{255} h(iT)s\{(k-i)T\}$$

If k = 0 is the time the last sample was taken and the echo estimate is required for k = 1 the equation reduces to;

$$e'(1T) = \sum_{i=0}^{255} h(iT)s\{(1-i)T\}$$

However, k = 0 is redefined every time a new sample is taken and e(1T) must be recalculated every sample period.

As already mentioned in Chapter 4 the method of realising this equation is simplified using logarithmic representation of speech samples s(kT) and filter coefficients h(kT). The final form in which the equation is;

$$e'(T) = \sum_{i=0}^{255} \text{antilog}\{\log(h(iT)) + \log(s((1-i)T))\}$$

A block diagram of the convolution board or digital transversal filter is shown in Fig. 7.10. Note the speech samples and filter coefficients are stored in solid state Random Access Memory and the antilogarithm is found by addressing a Programmable Read Only Memory (PROM) with the logarithm sum.

Once the filter coefficients are stored in memory (RAM) they remain in the same location until recalibration of the canceller occurs. The same 256 coefficients for h(iT) are, therefore, addressed in the same order for each

new echo estimate e'(T). Speech samples on the other hand are placed in RAM every sample period with the newest sample being placed in the location whose address is one less than that for the previous sample. The address counter being modulo 256 means that the next lower address below 0 is 255. This address counter is a down counter providing the address of the latest sample. This counter also forms the start address for an up counter which increments through 255 addresses for each new estimate. A diagram illustrating this process is found in Fig. 7.11.

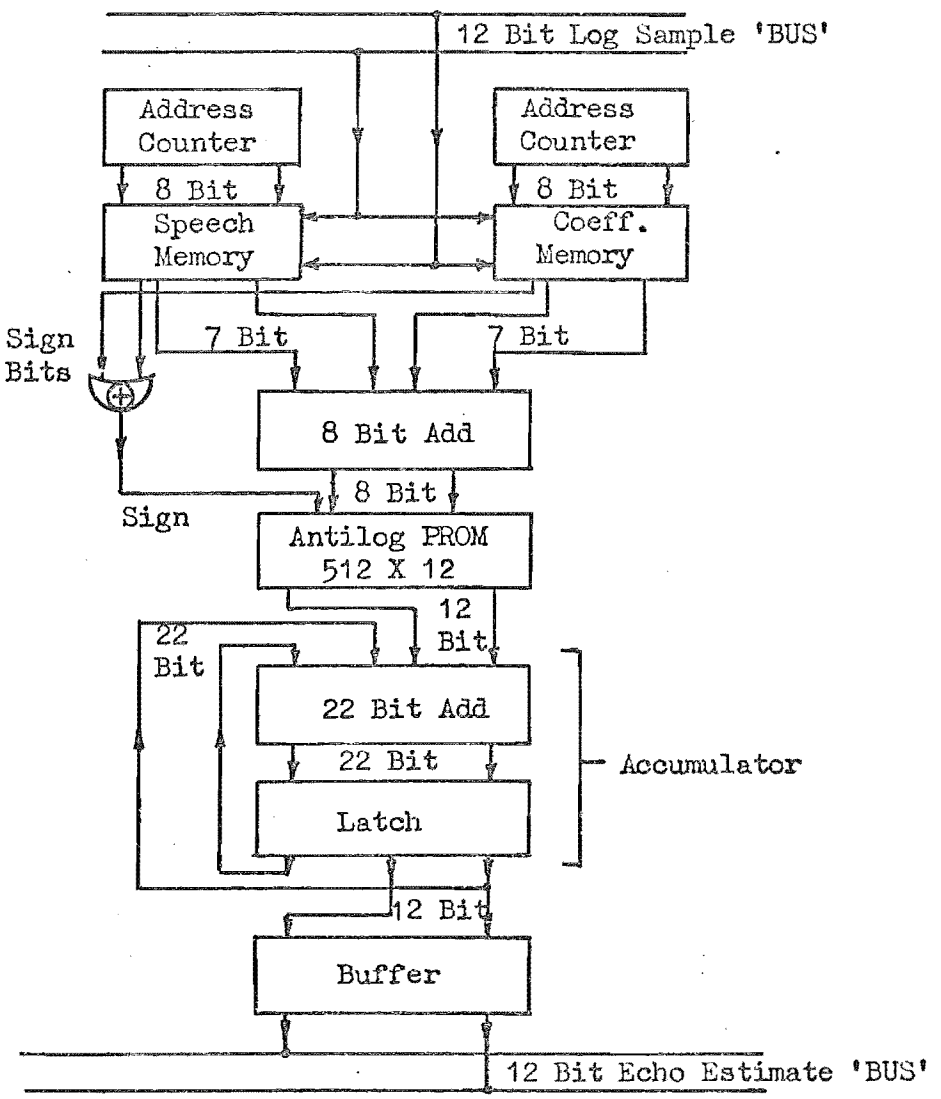


Fig. 7.10 Channel Convolution Circuitry

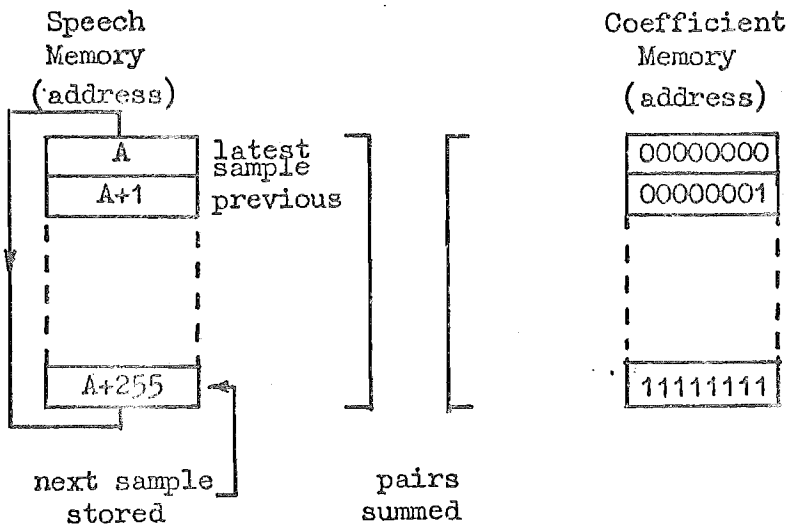


Fig. 7.11 Addressing of Speech Sample and Coefficients

The two 7 bit long magnitudes are summed and form an 8 bit output which along with the separate sign bit is held in a latch. If the sign bits of the two RAM output samples are different a negative product is indicated and this sign bit forms the 9 th address bit for the antilog PROM. The PROM is programmed to provide the two's complement for a negative product instead of generating it separately.

The linear products are accumulated and fed onto the echo estimate 'BUS' at the correct time for D/A multiplexed conversion.

The basic clock rate for the convolution process is 2.13 MHz with timing of the synchronised components being provided by a channel dedicated control board. The components synchronised to this clock are the up address counter, the two sets of latches with the buffer being synchronised

to the 8 KHz which is a sub-harmonic of 6.4 MHz. The 8 KHz channel timing is generated by a master timing circuit which staggers the 8 KHz timing to each channel for multiplex purposes. All timing connecting individual cancellers to a common 'BUS' is synchronised to these staggered 8 KHz clocks.

7.6 SYSTEM OPERATION

The inter-connection of all subsystems is best understood by following Fig. 7.12. The channel dedicated analogue board provides the necessary interfacing between the transmission circuit and other canceller boards. It provides either the speech or response waveform to the appropriate input on the multiplex board.

Each multiplex board selects one of 30 channels and converts it to digital representation to appear on the 12 bit linear 'BUS'. If a channel is under calibration the response samples appear on this 'BUS' otherwise speech samples appear. Speech samples are directly converted by the logarithmic converter but response samples are first used by the calibration circuit in the linear form.

The calibration circuitry adopts the timing of the channel under test and accepts the response samples off the 12 bit linear 'BUS'. The resultant filter coefficients are returned to the same 'BUS' and are converted by the logarithmic converter in place of the speech samples from that channel. These speech samples are prevented from appearing at this point during calculation of the coefficients.

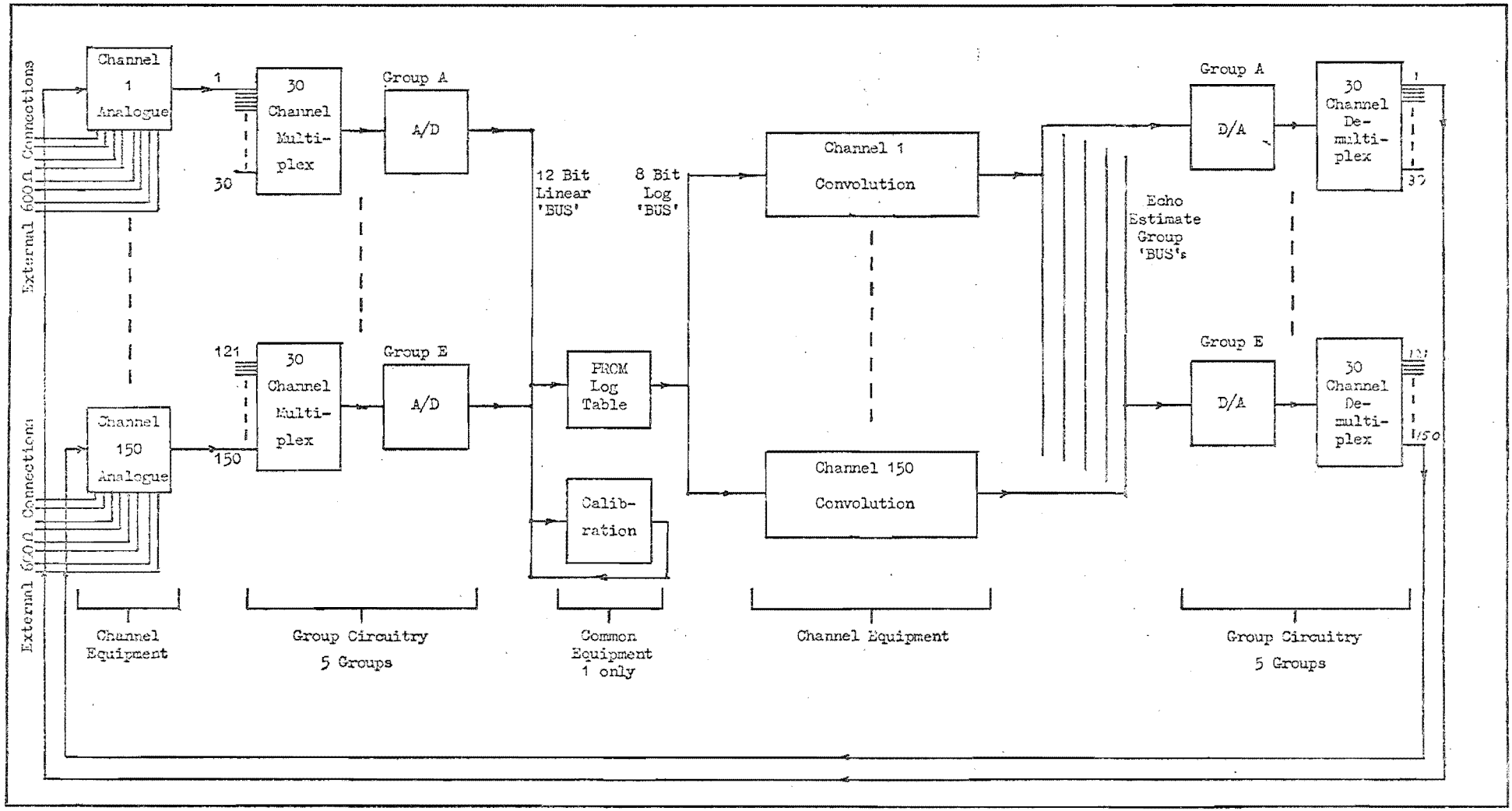


Fig. 7.12 Block Diagram of Complete System

The logarithmic converter takes the 12 bit linear values and converts them firstly to sign and magnitude and then to logarithmic format. The samples then appear on the 8 bit logarithmic 'BUS' to be used by the convolution board.

The convolution board stores speech samples in the speech memory or the filter coefficients in the coefficient memory during calibration. The echo estimate is generated and appears on the echo estimate 'BUS' in 12 bit linear form in 2's complement code.

The de-multiplex board provides D/A conversion at the appropriate time for each channel and analogue de-multiplexing. This board also provides for 30 channels and provides the echo estimate in analogue form for the analogue board. This estimate is only present for 3 uS, therefore, avoiding the errors arising from the Sin x/x roll off associated with the first order sample and hold circuit. Gain is provided by the analogue board to increases the energy contribution of the sample.

7.7 INTERIM TEST RESULTS

Although all circuitry has been completed and rack - mounted tests to date have been confined to single channel operation. Multiplex switching is by-passed and test results are only available for the calibration unit. The echo path has been modelled in bench tests using a 300 - 3000 Hz band-pass filter formed by cascading 8th order low-pass and high-pass butterworth filters.

The impulses obtained from the correlator have been compared with both the theoretical response of the filter and computer simulation of the hardware correlation of the echo path response as measured by the calibration circuit. The effect of using two level and three level sequences has also been demonstrated from the results of these tests.

The results obtained from the calibration circuit are compared with the theoretical case in Fig. 7.13. This is best compared with the magnitude spectrums of the impulse responses. The second and third plots show the differences in using the two level and three level pseudo noise sequences compared with the theoretical case in the first plot. The sin x/ x roll off characteristic of a first order sample and hold circuit and the two level sequence is clearly visible in the second plot. This is shown to be a characteristic of the transmitted sequence and not the echo path as the transmitted sequence is the only variation. If the two level sequence was used this weighting of the spectrum would be applied erroniously to the amplitude of the echo estimate.

A further plot showing the effect of having unequal positive and negative amplitudes of the three level sequence is shown in Fig. 7.14. The theoretical justification for this distortion can be understood by treating this error as the addition of a 1023 length train of rectangular pulses spaced at 125 uS intervals governed by the 8 KHz sampling rate.

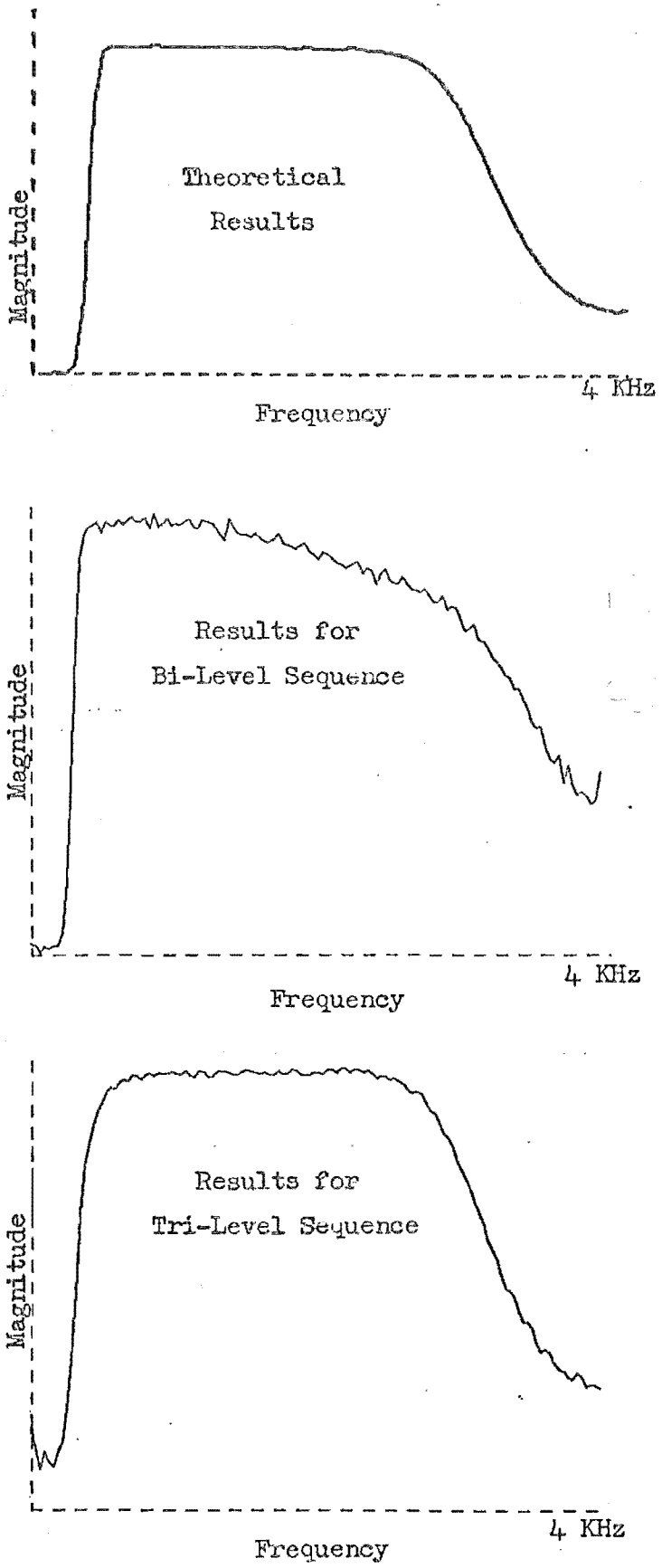


Fig. 7.13 Test Results for Correlation using Bi-level and Tri-level Sequences

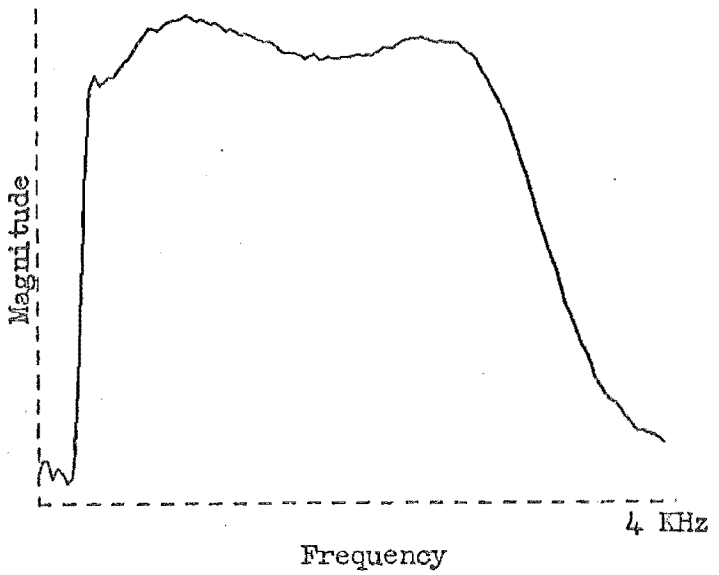


Fig. 7.14 Results for Tri-level Sequence when +ve and -ve Pulses are of Unequal Amplitude

CHAPTER EIGHT

SUMMARY

8.1 OVERVIEW

The aim of the project was to research the practicability of producing an echo canceller that would be economically viable and suitable for New Zealand conditions. Existing cancellers which are satisfactory under most conditions are a complex and expensive alternative to the conventional echo suppressor. These cancellers have shortcomings in that they rely on the presence of speech for adapting and this fails under double - talk or no - talk conditions, where any amount of phase roll is present. Where the rate of the phase roll exceeds 0.5 Hz they are totally unsatisfactory. For all these reasons echo cancellers are not widely accepted. By attempting to continually adapt to any time variance of the echo path, cancellers have become complex and expensive.

Fortunately, the New Zealand telephone network has very few instances of phase roll and this problem can be safely neglected. However, the problem was considered for academic reasons and proposals developed to demonstrate the feasibility of using a non-adaptive canceller as the heart of a phase tracking canceller. This then provides for wider

application of this less complex and, therefore, less expensive canceller design. It is envisaged that under phase roll conditions the basic canceller would be used until proved unsatisfactory, at which point a phase tracking circuit would be added. Such monitoring and control could well be achieved with a microprocessor based system.

8.2 THE SCALED 5 BIT CANCELLER

The original echo canceller designed at the University of Canterbury was constructed as an introduction to echo cancellation research. It was based on the principle that the simplest method to find the impulse response of the echo path was by direct measurement. The difficulty in multiplying digital values encouraged the use of the 5 bit word representation. The other characteristics of the design were the use of solid state Random Access Memory which proved very convenient, with the initial delay to the active period being incorporated in the memory addressing when reading signal samples.

By choosing a 5 bit representation and an analogue scaling technique, the +/- 15 levels were efficiently utilised. This involved adjusting the gain around the digital section of the transversal filter so as ideally the maximum signal sample and filter coefficients were represented by the maximum output of the A/D converter. This then reduced the quantisation error inherent in A/D conversion to be proportional to maximum value of each set of samples rather than the maximum possible value. This tended

towards a constant signal/noise ratio instead of what would otherwise be a constant quantisation noise. However, the range of this scaling was limited to 15 dB but this effectively represented an extra 2½ bits in the digital representation.

Tests showed that the canceller under ideal conditions provided cancellation of around 25 dB for constant level signals. Tests were of a limited nature and were carried out on a toll circuit between Auckland and Christchurch. However, they were sufficient to indicate those aspects of the canceller that were desirable. The convenience of the method of storage used provided a simple incorporation of the initial inactive delay period of the impulse response. This had previously been achieved in other cancellers by inserting a separate delay line. The practice of analogue gain scaling apart from being unsatisfactory for speech added complexity which was undesirable and unwarranted. By using a combination of both analogue and digital processing complexity was increased and the stability of the analogue gain adjustment circuitry was a problem. By the time testing of the canceller started its shortcomings were apparent and further developments and alternatives were being considered. The other major problem of circuit noise affecting the measurement of the impulse response was to be overcome by adopting pseudo random noise as an interrogation signal.

8.3 THE LOGARITHMIC CANCELLER

The changes of emphasis in this design reflected the

shortcomings and major areas of concern in the initial canceller. The analogue scaling was abondoned, and the problem of digital multiplication simplified by logarithmically coding the speech and impulse response samples. This true logarithmic conversion was achieved by addressing a Programmable Read Only Memory with the linear sample value, with the memory location holding the appropriate logarithmic value. This look-up table could be time shared over the full 150 channels, therefore, being a negligible cost.

The problem of system noise imposing itself on the filter coefficients with direct measurement was solved by using pseudo random noise as the interrogation signal and calculating the coefficients from the response. This effectively averages many direct impulse response measurements. A method of modifying the normal pseudo random binary sequence to provide a suitable interrogation signal proved very satisfactory. The result was to be able to measure the impulse response of the echo path with sufficient accuracy even in the presence of speech.

The problem of phase roll as it would affect this canceller has been discussed and a phase tracking circuit that could supplement this otherwise non-adaptive structure has been proposed.

The principle of using solid state Random Access Memory as incorporated initially in the original canceller has been maintained. The original technique of using only

the 64 active filter coefficients was considered to be marginally unwarranted. The complexity in determining this initial period was not considered to outweigh the need to lengthen the convolution to the full 256 summation. The only possible reason to return to the 64 length convolution is to reduce the noise contribution by the other 192 coefficients. By putting these other coefficients to zero that small amount of noise produced by speech being present during calibration would be reduced by 6 dB, i.e. the error noise power would appear only in the 64 coefficients and not 256.

Although time did not permit the testing of the complete canceller the results of tests on the calibration circuitry prove the validity of the calibration technique used. The use of 8 bit logarithmic coding giving a constant signal to noise ratio, 12 bit linear coding giving a low idle noise and the direct calculation of the impulse response samples are considered to be sound. Although the correlation necessary to achieve the filter coefficients is long it is not complex and is cost effective when used for the calibration of many channels.

The overall view is of a canceller that is relatively simple and with the time sharing of the expensive and bulky components should provide an attractive alternative to the suppressor. With channel dedicated components being primarily digital memory, adders, buffers, logic and analogue amplifiers, the component cost is low.

8.4 HINDSIGHT

Although much has been achieved in the design and construction of the first canceller and the subsequent development of the later design, some problems are still being experienced in eliminating the remaining detailed technical problems. With hindsight it is not difficult to see how some of these problems may have been minimised.

The confidence in being able to do justice to design, construction, testing as well as theoretical research into such areas as system identification and phase tracking may have been overly optimistic. Although the theoretical research did not directly conflict with the desirability of producing a working canceller it consumed effort which may have been more productive. This distribution of effort may have contributed to incomplete aspects of either the theoretical work or hardward design, construction and testing.

Designing and constructing hardware in a University atmosphere without the backing of an experienced technical team dedicated to that particular project is a handicap. Although capable technician assistance was utilised this was on a casual basis where continuity or deep involvement were not possible. This meant all detailed design was my sole responsibility leaving little opportunity for the discussion of detailed technical problems.

The decision to proceed with a multiplex design instead of an individual canceller prior to proving these

particular techniques was unwise. As the multiplexing is based on standard practices this could easily have been theoretically justified at a later date.

With the above reservations I am satisfied with the progress made. The construction of the first canceller was entirely satisfactory and the development of the principles behind the later one appear sound. The tests that have been completed on the later canceller give reason for confidence.

8.5 THE FUTURE

As my association with the University terminates and my attention, if only temporarily, turns to other responsibilities, the New Zealand Post Office must now take responsibility for the future of this canceller. It is important that the effort and financial commitment given this project be rewarded by a proper evaluation of the design. It is unfortunate that this has not been possible to date.

Although all circuit boards have been completed and rack mounted some technical faults need to be eliminated prior to final bench and circuit tests. The calibration circuit, however, is complete and works satisfactorily and in itself may have application in system identification in the Post Office.

The future of the canceller beyond this stage will depend on the feasibility of having a canceller constructed

specifically for New Zealand conditions. The advantages of standardisation must also be considered if and when cancellers become widely used. If the canceller proves satisfactory for New Zealand conditions the decision will be made not only on the above criteria but on the economic factor. If the proposed phase tracking technique proved satisfactory it could well be that such a design could have wider application.

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APPENDIX I

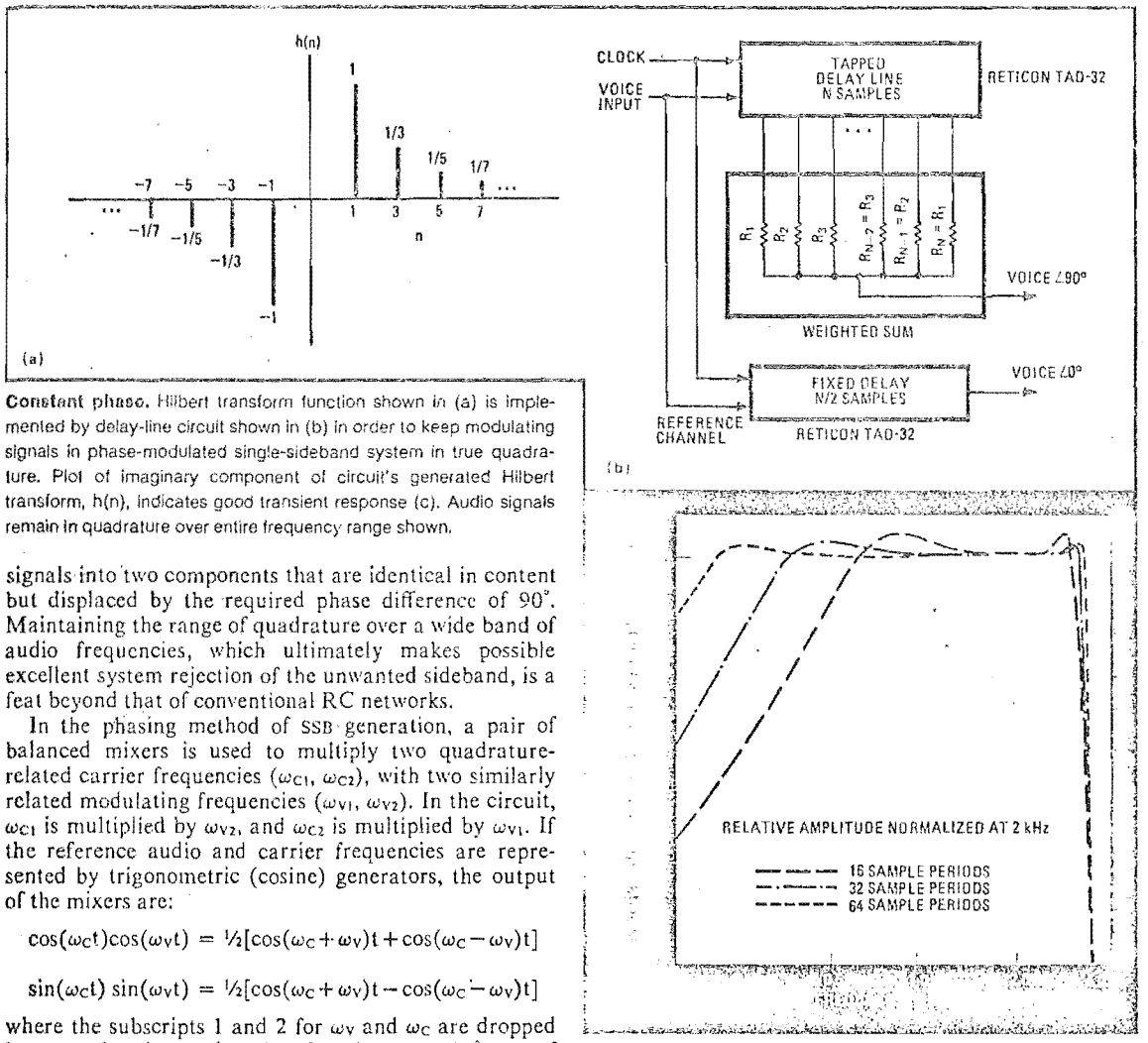
REPRINTS OF PAPERS PUBLISHED OR SUBMITTED BY THE AUTHOR ON SUBJECTS RELATING TO THIS THESIS

Delay lines help generate quadrature voice for SSB

by Joseph A. Webb and M. W. Kelly
University of Canterbury, Christchurch, New Zealand

The major difficulty faced by designers when trying to generate a single-sideband signal by the phase-shift method—that is, obtaining the modulating signals in quadrature over a wide band while achieving good transient response—may be overcome by implementing the well-known Hilbert transform with two clocked analog delay lines and a resistor weighting network.

This simple circuit splits the modulating (audio)



Constant phase. Hilbert transform function shown in (a) is implemented by delay-line circuit shown in (b) in order to keep modulating signals in phase-modulated single-sideband system in true quadrature. Plot of imaginary component of circuit's generated Hilbert transform, h(n), indicates good transient response (c). Audio signals remain in quadrature over entire frequency range shown.

signals into two components that are identical in content but displaced by the required phase difference of 90°. Maintaining the range of quadrature over a wide band of audio frequencies, which ultimately makes possible excellent system rejection of the unwanted sideband, is a feat beyond that of conventional RC networks.

In the phasing method of SSB generation, a pair of balanced mixers is used to multiply two quadrature-related carrier frequencies (ω_{C1}, ω_{C2}), with two similarly related modulating frequencies (ω_{V1}, ω_{V2}). In the circuit, ω_{C1} is multiplied by ω_{V2}, and ω_{C2} is multiplied by ω_{V1}. If the reference audio and carrier frequencies are represented by trigonometric (cosine) generators, the output of the mixers are:

$$\cos(\omega_C t)\cos(\omega_V t) = \tfrac{1}{2}[\cos(\omega_C+\omega_V)t+\cos(\omega_C-\omega_V)t]$$

$$\sin(\omega_C t)\sin(\omega_V t) = \tfrac{1}{2}[\cos(\omega_C+\omega_V)t-\cos(\omega_C-\omega_V)t]$$

where the subscripts 1 and 2 for ω_V and ω_C are dropped because the sine and cosine functions are 90° out of phase. The output of each mixer is then added or subtracted to obtain the upper ($\omega_C+\omega_V$) or lower ($\omega_C-\omega_V$) sideband, as desired. Remember, however, that quadrature between the audio and carrier frequencies must be maintained for optimum response.

The discrete Hilbert transform of any signal, that is:

$$h(n)=\frac{1-e^{j\pi n}}{\pi n}=\frac{1-\cos\pi n}{\pi n}$$

corresponds to a 90° phase shift of all its frequency components, and thus by implementing this function the quadrature relationship for the audio channels is maintained. Attaining quadrature for carrier signals is simple, since the ω_C signal has virtually zero bandwidth.

The discrete Hilbert transform is defined from plus to minus infinity, although truncation is needed for physical realization of the function. The truncated impulse response of this function is illustrated in (a).

The required response may be generated with the delay-line circuit shown in (b). A Reticon TAD-32 charge-coupled device is used for the delay line. The weighting resistors are selected so that the circuit will generate the product of the truncated function, h(n), and a smoothing or weighted function, W(n), where $W(n)=\cos^2 n\pi/N$. Each resistor is selected so that $R(n)=h(n)W(n)$. Note that the $\cos^2$ function is defined from +90° to −90°, not from plus to minus infinity.

The reference voice channel is delayed by N/2 samples for the audio channels to remain in true quadrature. At a clock frequency of 8 kilohertz, the delay amounts to 4 milliseconds for 64 samples.

The plot of the imaginary component of h(n) in (c) of the figure illustrates the excellent transient response of the circuit. As can be seen, relatively few samples are needed for good performance. In these tests, the clock frequency was 8 kHz. For telephone-quality voice signals, N = 32 is sufficient, and N = 64 represents excellent performance. Since the Hilbert transform is symmetrical, that is, $f(t)=-f(t)$, quadrature is perfect over the entire frequency range shown. □

TELEPHONE ECHO CANCELLATION FOR SATELLITE TERMINALS

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University of Canterbury
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ABSTRACT

ECHOES OCCUR IN A TELEPHONE CHANNEL AT THE HYBRID TRANSITION FROM 2-WIRE TO 4-WIRE CIRCUITS. UNTIL RECENTLY THESE ECHOES HAVE BEEN IGNORED, BUT TIME DELAY IN LONG DISTANCE CALLS, AND ESPECIALLY IN SATELLITE CALLS, MAKES OTHERWISE ACCEPTABLE LEVELS OF ECHOES PARTICULARLY OBJECTIONABLE. A NUMBER OF DEVICES HAVE BEEN DESIGNED IN RECENT YEARS TO SUPPRESS OR CANCEL THESE ECHOES. AT THE UNIVERSITY OF CANTERBURY, IN COOPERATION WITH THE NEW ZEALAND POST OFFICE, WE HAVE DESIGNED A VERY SIMPLE ECHO CANCELLER. WE HAVE USED A 5 BIT WORD, COMPARED TO 8 BITS USED IN MOST DEVICES, WITHOUT SACRIFICE IN PERFORMANCE. A SINGLE IMPULSE LEARNING PROCEDURE IS USED TO COVER THE ENTIRE BANDWIDTH, COMPARED WITH THE MUCH MORE COMPLEX CORRELATIVE LEARNING PROCEDURES USED IN MOST SYSTEMS. A MORE ADVANCED SYSTEM NOW UNDER CONSTRUCTION USES A PSEUDORANDOM NOISE SEQUENCE FOR LEARNING, AND A LONGER WORD LENGTH, BUT IT STILL RETAINS MOST OF THE FEATURES OF SIMPLICITY CHARACTERISTIC OF THE EARLIER SYSTEM.

TELEPHONE CIRCUITS

Local telephone connections are made on bidirectional pairs of wires. This means a physical connection between two subscribers on which speech travels in both directions. Between main centres, and for distances greater than about 50 miles, communication is by means of two separate unidirectional circuits. Local bidirectional circuits between the subscriber and his exchange are termed 2-wire circuits, and unidirectional circuits between more distant exchanges are referred to as 4-wire. Also, 4-wire circuits are used on all long distance calls and on international calls either by cable, radio, or satellite link.

With 4-wire circuits between exchanges and 2-wire circuits locally, some form of interfacing is required between the two types of circuit. This is achieved at each subscriber's local exchange by means of a "hybrid" transformer. This transformer has three ports, one for each half of the 4-wire circuit, and one for the 2-wire circuit. The transformer permits energy to pass from the incoming 4-wire circuit to the 2-wire port, and the energy coming into the 2-wire port to pass to the outgoing 4-wire circuit. Ideally all energy is transferred in this manner, but like other things, hybrids cannot be perfectly matched, and incoming lines are frequently very poorly matched. As a result, echoes are generated at the hybrid by the impedance mismatch. Typical echoes are about -8 db with respect to the outgoing signal, but they can be as high as -4 db and still be within specifications.

Figure 1 shows a block diagram of the local/national telephone network, with 2-wire to 4-wire transitions, and relative signal levels at various points. Figure 2 shows typical hybrid signal levels and the interconnecting ports.

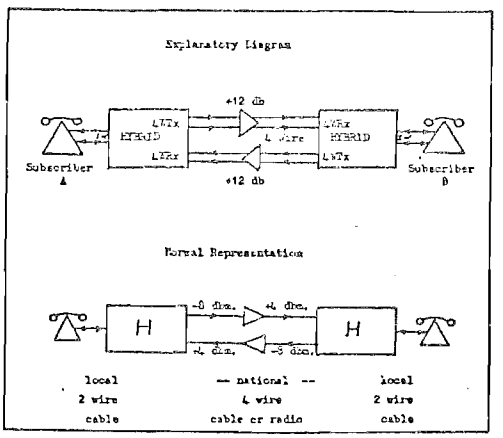

Figure 1: Block diagram of the local/national telephone network.

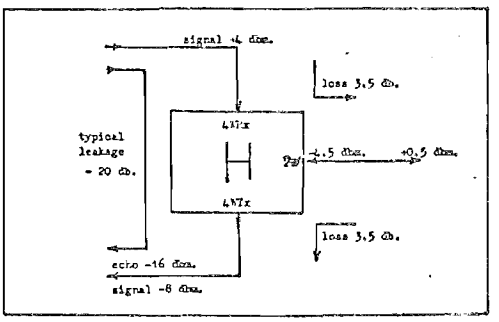

Figure 2: Block diagram showing typical hybrid signal levels, and the interconnecting ports.

EFFECT OF DELAY ON ECHOES

Echoes have always been present on national telephone circuits, but it is only in cases of extreme delay that this presents a problem. If the round trip delay of an echo is less than 50 mS, then little problem is experienced on the line. About 30 mS is the maximum round trip delay within New Zealand, but considerably greater delays may be experienced in larger countries such as the United States and Australia, particularly when the connection is routed along non-direct paths.

Where a satellite link is used in a telephone circuit, delays in excess of 400 mS per satellite "hop" makes delay interference extremely serious. Figure 3 is a block diagram of a satellite linked telephone circuit, showing about 120 mS delay to the satellite, giving a total circuit round trip delay of about 480 mS, plus the delay in the national circuit. Since annoyance due to echoes increases with delay, as shown in figure 4, a

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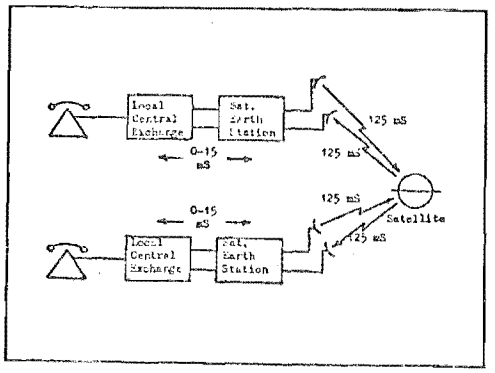


Figure 3: Satellite linked telephone circuit.

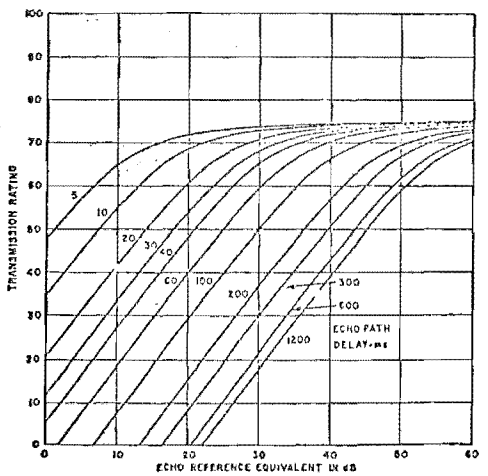


Figure 4: Transmission rating vs delay in a telephone network (from CCITT 6529).

satellite link is the worst case of all.[1]

ECHO SUPPRESSORS

An early method of overcoming echo problems was to insert a loss in the 4-wire return path when an outgoing speech was detected. This circuit was called an echo suppressor. While some success was experienced with this method in national circuits, its performance on satellite circuits was less than satisfactory as reported by Rosenberger and Thomas.[2] A block diagram of an echo suppressor is shown in figure 5.

Operation of an echo suppressor depends upon a fixed loss, which is switched into the suppressed direction of the 4-wire circuit, while the dominant direction maintains control. Inserted loss is normally 50 db. Switching between dominant directions sometimes results in speech mutilation called "chopping", and in reversion to duplex operation. In reversion to duplex operation, echoes again appear.

Echo suppressors are not very satisfactory in satellite circuits, due to the delay. This extra delay causes confusion, and an increase in "double talking". As the echo suppressor relies on an

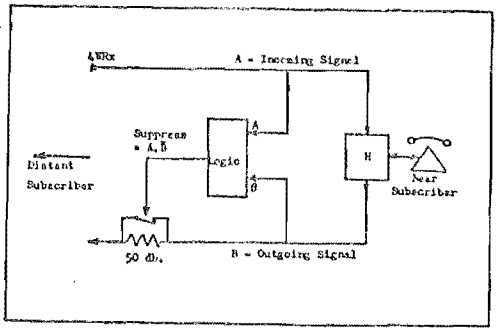


Figure 5: Echo suppressor operation.

absence of double talking, its effectiveness is significantly reduced.

ECHO CANCELLERS

Due to the shortcomings of the echo suppressor on satellite circuits, echo cancellers were developed. In this approach, the echo is actually cancelled from the circuit, rather than suppressed. A transversal filter models the characteristics of the echo path, then cancels the echo based on these characteristics. A block diagram of an echo canceller is shown in figure 6.

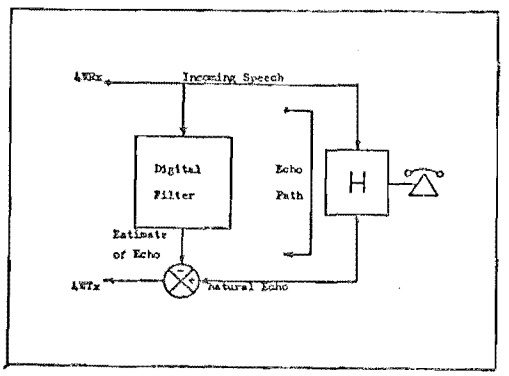


Figure 6: Echo canceller operation.

EXPECTED ECHO LEVELS

A comprehensive study of echo characteristics reported by CCITT in 1975 forms a good basis for determining these requirements.[3] Although these tests were carried out on the French telephone network, the relevant information is fairly generally applicable, although the total delay in the response will be a function of the size of the country involved. These test results show a mean echo transfer attenuation of 13.6 db, with a standard deviation of 5.1 db.

Study of the impulse response characteristics of the network formed the basis of the report on the French network. If an impulse function is placed on the line, this is followed by a fixed delay and finally an active period of the response. These tests showed that the active period, containing greater than 99.95% of the impulse reflected energy, was confined to an 8 mS period. From these figures, if a sampling rate of 8 KHz is assumed, then a total

of 64 samples is required to represent the active period of the response. Total time delay to the active period will vary considerably, but in New Zealand it is not expected that this period will exceed 32 mS. Another report[4] shows that the peak of the response will occur within 0.5 mS of the beginning of the active period. This was found to be important in the design of our echo canceller.

TESTS ON NEW ZEALAND CIRCUITS

To ensure that the characteristics of New Zealand circuits were similar to those reported for the French network, tests were carried out on several circuits between Christchurch and Auckland (about 500 miles, 800 km).

A 5 microsecond rectangular pulse of high amplitude was used for these tests to simulate an impulse function. To overcome Post Office objections to a high amplitude pulse, and to increase the amount of energy in the bandwidth, the pulse was bandpass filtered prior to connection to the line. This meant that a filtered pulse could be transmitted with peak amplitude equivalent to the peak "test tone" level of -8 dlm. The resultant echoes are shown in figure 7 for several different line terminations at Auckland. Note that high frequency echoes are delayed somewhat more than the lower frequencies.

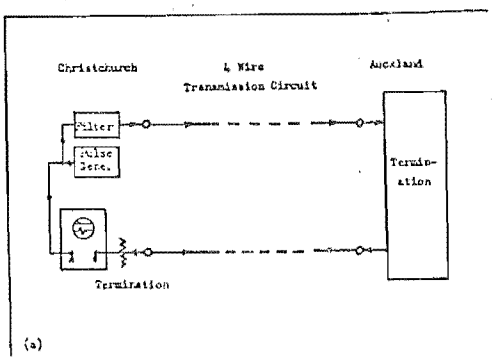
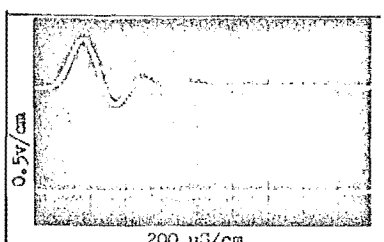
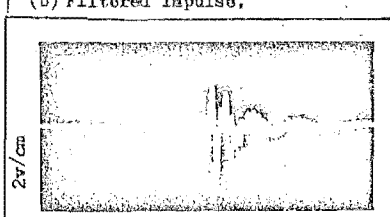


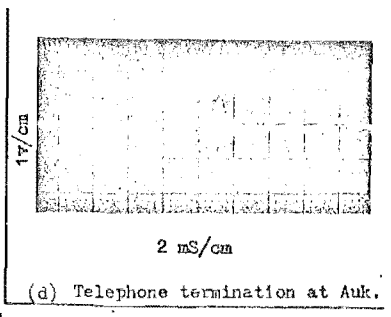
Figure 7(a) Christchurch-Auckland test circuit.



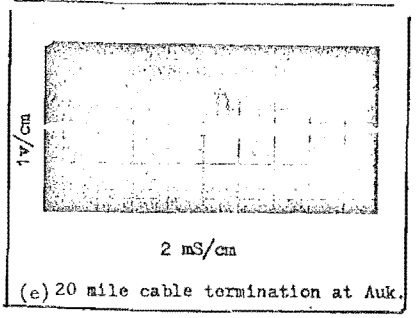
(b) Filtered impulse,



(c) Hybrid replaced by 12 db pad



(d) Telephone termination at Auk.



(e) 20 mile cable termination at Auk.

ECHO TESTS IN AN AUDITORIUM

Although it is not directly related to the problem of telephone echo cancellation, the use of the same cancellation techniques to reduce the feedback present in public address systems presents some interesting possibilities. In this case, cancellation creates a "dead zone" in the vicinity of the microphone. Another possibility is to create the "perfect" auditorium at all points by means of echo generation rather than cancellation.

The Ngiaio Marsh Theatre at the University of Canterbury was used as a "typical" auditorium for these tests. A block diagram of the test circuit is shown in figure 8(a), and the resultant impulse response in (b). Approximately 90% of the energy occurs in the first 200 mS. Since these tests were made in an unloaded (empty) auditorium, greater damping (shorter response) could be expected in a loaded auditorium, giving better results.

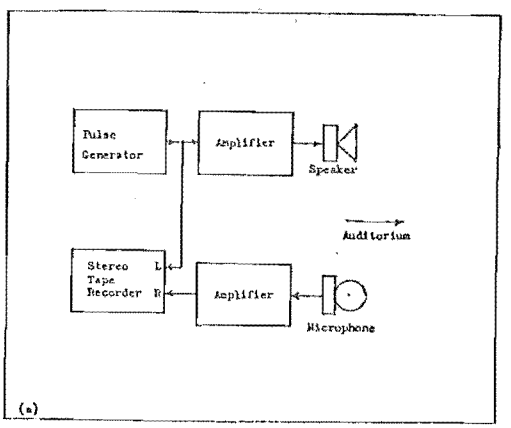
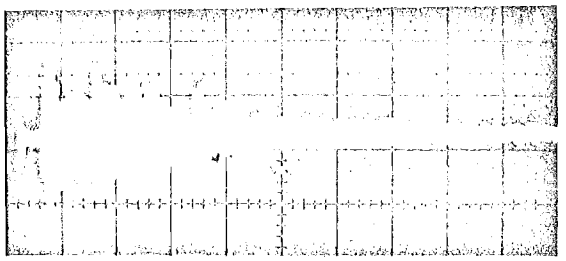


Figure 8(a) Auditorium test circuit.



(b) Impulse response of auditorium (50 mS/cm)

THE DIGITAL FILTER AS AN ECHO CANCELLER

By storing a sampled version of the impulse response, and by sampling the transmitted signal, discrete convolution of these functions can be used to generate the expected echo for cancellation purposes. This technique is called transversal filtering.

Although virtually all echo cancellers use transversal filters, there are significant differences in the detailed designs[5,6,7,8]. Many of the results of the performance of these cancellers is published by COMSAT[7], in the form of field trial results on echo cancellers and echo suppressors. Typical results show 21 db to 25 db of echo cancellation, which is quite satisfactory for most purposes. Since this report was written, some echo cancellers have been designed showing even better performance.

UNIVERSITY OF CANTERBURY DESIGN

It has already been mentioned that we decided to use a simple impulse response learning procedure, rather than the more complex correlative learning procedure used in most echo canceller designs. We had also decided to use only 5 bits in our design, since this simplified the calculations considerably. Additional departures were made from convention, the following being the major innovations:

1. RAM's were used to store the impulse response, and an accessing arrangement was designed so that only the "active" period of the response was used.
2. The impulse response and the signal samples were scaled by a digital AGC system, so that full use could be made of the 5 bit samples. Echo cancellation was therefore scaled to the pre-cancellation echo level, rather than to the signal (voice).
3. A 256 x 8 PROM (2048 bits) was used as a simple lookup table to perform multiplication of the 2 4 bit words, while bypassing the sign bit of the 5 bit words. This procedure served to greatly simplify the design.

Our echo canceller operates by switching between "calibrate" and "operate" modes. Although it is completely flexible in programming of these modes, the scenario goes something like the following:

1. When the line connection is established, a single impulse is transmitted to calibrate the channel. With the impulse response constants properly stored, the echo canceller is then switched to "operate".
2. The system remains in "operate" mode until such time as external (correlative, but extremely simple) measurements show that echo cancellation is no longer effective.
3. On command, the system switches back to "calibrate" followed by reversion to "operate". Regular polling of all channels is done periodically by means of this external circuitry.

Single point correlation procedures will be used on each channel to determine the performance of the canceller on a continuous basis. When a canceller is sufficiently out of specification it will be "flagged", and recalibrated on the next poll.

Figure 9 is a bench test curve run to determine the effectiveness of this canceller. Since the maximum theoretical cancellation for a 5 bit system is 30 db, we were very pleased with these results. Figure 10 shows the results of testing this device on the Christchurch-Auckland telephone circuit. Although these results were not quite as good as the bench tests, this was due chiefly to the practical problems of interfacing with the line, rather than any inherent system limitations. Also, we were not especially anxious to spend very much time improving this system, since we were impatient to get going on our new improved system.

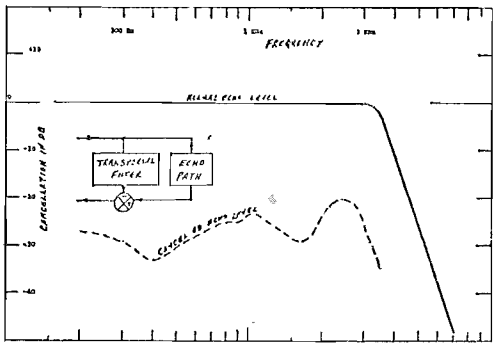


Figure 9: Performance of the University of Canterbury echo canceller in bench tests.

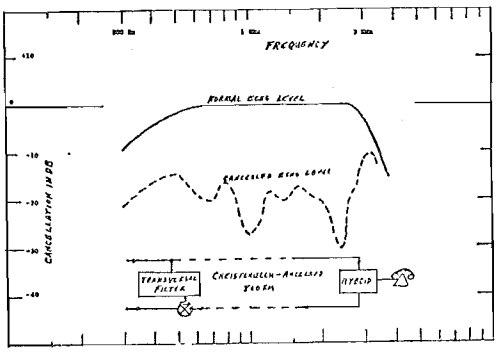


Figure 10: Performance of the University of Canterbury echo canceller on a Christchurch-Auckland telephone circuit.

LOOKING AHEAD

Having demonstrated to our own satisfaction the viability of this echo cancellation technique, we have now abandoned this system and proceeded towards the design of a more advanced model. In the more advanced model we have eliminated the single impulse learning procedure in favour of a pseudorandom noise burst sequence. This PRN burst lasts for about 100 mS, and sounds like a subdued scratch or hiss. Even during active speech the PRN burst does not interfere with speech, and even more importantly,

active speech does not interfere with our PRN burst. By averaging, the PRN burst gives excellent accuracy on the filter constants. Simple correlation and polling is still used in this system to determine if and when recalibration is needed.

We are also using a greater word length and digital companding in our advanced model. This is done not so much to reduce quantizing noise, as to simplify certain word handling procedures.

The most important point in the more advanced model is that we have taken a systems engineering approach, so that this canceller can operate in a "bank" of cancellers, supervised by a microprocessor. The microprocessor will do all mode switching, performance monitoring, and supervision. We are also analysing and making provisions for "phase roll" problems, which is so difficult for most echo cancellers to handle. Phase roll provisions will not be made on every echo canceller, however, as this requires some special design features.

Phase roll occurs due to slight frequency offset in non-synchronised oscillators used in SSB/FDM systems in some telephone networks. Although no such problems exist in the New Zealand telephone network, it is a very significant problem overseas, and we think we have a quite unique approach to its solution.

Construction is almost complete on our new canceller, and bench and field tests are beginning. Before the end of 1978 we expect all tests to be complete, and these will include satellite tests from our only New Zealand satellite terminal at Walkworth, north of Auckland. We expect maximum echo cancellation of about 40 db, from design projections.

ACKNOWLEDGEMENT

The authors are especially grateful to Mr. Rob B. Wilkinson, Division Engineer (Transmission), New Zealand Post Office, Wellington, for his able assistance and encouragement.

The foregoing sounds like an ordinary acknowledgement, but we intend it as much more. Rob suggested this project in the first place. He offered design ideas and criticisms, keeping us continuously abreast of the latest design data, particularly in the telephone literature which is not generally available. Even though he has a very busy schedule, he has always made himself available by telephone and personal contact when needed. He has the extraordinary talent of combining advanced vision with practical methods of getting the job done. In this and other research projects in telecommunications at the University, Rob has contributed very generously in time and in talent, for which we are truly grateful.

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AN IMPROVED ECHO CANCELLATION TECHNIQUE

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ABSTRACT

In cooperation with the New Zealand Post Office, we have designed a telephone echo canceller with a number of original features. Among these are the following:

(a) A pseudorandom sequence is used to calibrate the channel and provide constants for the transversal filter. Correlation is used only as a check to determine if any changes have taken place in the channel which requires transmission of a second binary sequence.

(b) Logarithmic companding is used to reduce noise, reduce storage requirements, and to simplify arithmetic computations.

A pseudorandom binary sequence is transmitted along the channel when the connection is initially made. It sounds like a subdued scratch, and although it is done when voice is not ordinarily on the line, it does not interfere significantly with voice intelligibility even if transmitted during active conversation, and voice does not materially effect the validity of the measured constants.

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TELEPHONE CIRCUITS

Local telephone connections are made on bidirectional pairs of wires. This means a physical connection between two subscribers on which speech travels in both directions. Between main centres, and for distances greater than about 50 miles, communication is by means of two separate unidirectional circuits. Local bidirectional circuits between the subscriber and his exchange are termed 2-wire circuits, and unidirectional circuits between more distant exchanges are referred to as 4-wire. Also, 4-wire circuits are used on all long distance calls and on international calls either by cable, radio, or satellite.

With 2-wire circuits serving the local area and 4-wire circuits between main centres, some form of interfacing is required. This is achieved at the local exchange by means of a "hybrid" transformer. The hybrid transformer is a directional coupler with three ports, one for each half of the 4-wire circuit, and one for the 2-wire circuit. The hybrid permits energy to pass from the incoming 4-wire circuit to the 2-wire port, and the energy coming into the 2-wire port to pass to the outgoing 4-wire circuit. Ideally all energy is transferred in this manner, but like other things, hybrids cannot be perfectly matched, and incoming lines are frequently very poorly matched. As a result, echoes are generated at the hybrid by the impedance mismatch. Typical echoes are about -8 db with respect to the outgoing signal, but they can be as high as -4 db and still be within specifications.

Figure 1 shows a block diagram of the local/national telephone network, with 2-wire to 4-wire transitions, and relative signal levels at various points. Figure 2 shows typical hybrid signal levels and the interconnecting ports.

EFFECT OF DELAY ON ECHOES

Echoes have always been present on local and national telephone circuits, but it is only in cases of extreme delay that this presents a problem. If the round trip delay of an echo is only a few milliseconds, then

little problem is experienced on the line. About 20 mS is the maximum round trip delay within New Zealand, but considerably greater delays may be experienced in larger countries such as the United States and Australia, particularly when the connection is routed along non-direct paths.

Where a satellite link is used in a telephone circuit, delays in excess of 500 mS makes delay interference extremely serious. Figure 3 is a block diagram of a satellite linked telephone circuit, showing about 125 mS delay. Round trip delay for each subscriber therefore is about 500 mS for him to hear his own voice reflected. Figure 4 shows how quickly the transmission quality is degraded by delay in the echo.[1]

ECHO SUPPRESSORS

An early method of overcoming echo problems was to insert a loss in the 4-wire return path when any outgoing speech was detected. This circuit was called an echo suppressor. While some success was experienced with this method on national circuits, its performance on satellite circuits was less than satisfactory as reported by Rosenberger and Thomas.[2] A block diagram of an echo suppressor is shown in figure 5.

Operation of an echo suppressor depends upon a fixed loss, which is switched into the suppressed direction of the 4-wire circuit, while the dominant direction maintains control. Inserted loss is normally 50 db. Switching between dominant directions sometimes results in speech mutilation called "chopping", and in reversion to duplex operation, where echoes again appear.

ECHO CANCELLERS

Due to the shortcomings of the echo suppressor on satellite circuits, echo cancellers were developed. In this approach, the echo is actually cancelled from the circuit, rather than suppressed. A transversal filter models the characteristics of the echo path, then cancels the echo based on these characteristics. A block diagram of an echo canceller is shown in figure 6.

EXPECTED ECHO LEVELS

A comprehensive study of echo characteristics reported by CCITT in 1975 forms a good basis for determining these requirements.[3] Although these tests were carried out on the French telephone network, the relevant information is fairly generally applicable, although the total delay in the response will be a function of the size of the country. These tests show a mean echo transfer attenuation of 13.6 db, with a standard deviation of 5.1 db.

Study of the impulse response characteristics of the network formed the basis of the report on the French network. If an impulse function is placed on the line, this is followed by a fixed delay and finally an active period of the response. These tests showed that the active period, containing greater than 99.95% of the impulse reflected energy, was confined to an 8 mS period. From these figures, if a sampling rate of 8 KHz is assumed, then a total of only 64 samples is required to represent the active period of the response. Total time delay to the active period will vary considerably, but in New Zealand it is not expected that this period will exceed 20 mS. Another report shows that the peak of the response will occur within 0.5 mS of the onset of the active period.[4]

TESTS ON NEW ZEALAND CIRCUITS

To ensure that the characteristics of New Zealand circuits were similar to those reported for the French network, tests were carried out on several circuits between Christchurch and Auckland (about 500 miles, 800 KM). A 5 microsecond rectangular pulse was used for these tests to simulate a Dirac impulse function. Figure 7 shows the results of these tests.

ECHO CANCELLER DESIGNS

There are very significant differences in the various designs of echo cancellers.[5,6,7,8] Many of the results of canceller performances have been published by COMSAT.[9] Typical results show 21 db to 25 db of echo cancellation, which is quite satisfactory for most purposes. Some of the newer designs show even better performance.

All echo cancellers use transversal filters for achieving echo cancellation, and almost all use correlative learning procedures to measure the constants for the transversal filters. Although this is in general a very satisfactory technique, correlative learning has certain disadvantages, as follows: (a) learning can only be achieved when there is signal present on the line, (b) learning is sometimes slow, and (c) recent tests show what appears to be a "random walk" of changing constants propagating through the transversal filter, due to the continuous learning process.

Inspired by the simplicity of the Dirac impulse function for measuring transversal filter constants, where the impulse response samples themselves are the filter constants, we decided to design an echo canceller based on this principle. Using a 5 microsecond pulse followed by a multipole low pass filter with a cutoff frequency just outside the telephone bandwidth, we designed a simple but effective echo canceller which gave 25 db to 30 db across the voice bandwidth, as reported in a previous publication.[10]

Although the Dirac impulse function is ideal theoretically, and even though it can be simulated quite well by means of a narrow bandwidth pulse, it suffers the disadvantages that (a) a sudden impulse does not sound very good on a telephone line, and (b) it is difficult to obtain sufficient power in the impulse function to give reliable and accurate transversal filter constants.

A truncated pseudorandom binary sequence on the other hand can be made to overcome both of these difficulties, while yielding the same constants with only moderately increased complexity. The PRN sequence sounds like a pleasant subdued hiss on the line, while yielding greatly increased AVERAGE power which can be convolved into an impulse function very similar to that of the Dirac impulse.

TRUNCATED PRN SEQUENCE

To obtain the impulse response of a channel, a PRN sequence is transmitted along the channel such that, when the response of the channel is correlated with a modified version of the interrogation sequence, the impulse response results. Figure 8 shows a continuous PRN binary sequence of length PT, which correlates into an impulse function

of width 2T, where T is the clock period.[11]

The autocorrelation is a repetitive function however, and approximates an impulse function only as P is increased or as the number of repetitive sequences transmitted is increased. To avoid a continuous transmission of the sequence, we have discovered that we can use an extended version of the original sequence for correlation purposes, as long as the extended sequence is equal to the transmitted sequence plus twice the length of the transient response of the channel.

As the impulse response is required to be known for a digital transversal filter, only values at discrete time intervals of T are required, rather than as a continuous function, where 1/T is the clock rate of the discrete system. Furthermore these will be calculated from the system response sampled at intervals of T. All correlations and convolutions considered will be discrete time processes.

Let S(KT) be a discrete representation of the interrogation signal, being one cycle of a pseudo random binary sequence of length P; i.e. S(KT) is non-zero only for $0 \leq K < P$. Also let the discrete impulse response h(KT) be known to exist for $0 \leq K < L$.

The response of the channel to S(KT) is r(KT) and is necessarily confined to the time period $0 \leq K < P+L$. Let S'(KT) be an extended version of S(KT) such that the cross correlation of these two functions approximates a delta function over the time period of interest.

The discrete response r(KT) is given by the discrete convolution of the transmitted signal S(KT) and the impulse response h(KT), plus any noise present at the time (Note: If speech is present on the channel at the time of measurement, it is considered as noise).

$$r(KT) = \sum_{i=0}^{L} S\left[(K-i)T\right] h(iT) + n(KT) \qquad (1)$$

The cross correlation of r(KT) and the function S'(KT) which is required to give the impulse response $\gamma h(KT)$ is given by:

$$\gamma_{S'r}(KT) = \sum_{j=0}^{P+L} S'\left[(K+j)T\right] r(jT) \qquad (2)$$

Summation over the limited range r(jT) is non-zero only for $0 \leq j < P+L$.

Substituting for r(KT) in (2):

$$\varphi_{S'r}(KT) = \sum_{j=0}^{P+L} S'\left[(K+j)T\right] \sum_{i=0}^{L} S\left[(j-i)T\right] h(iT) + \sum_{j=0}^{P+L} S'\left[(K+j)T\right] n(jT) \quad (3)$$

Introducing the variable $\lambda = j-i$

$$\varphi_{S'r}(KT) = \sum_{\lambda=-i}^{P+L-i} S'\left[(K+i+\lambda)T\right] \sum_{i=0}^{L} S(\lambda T) h(iT) + \sum_{j=0}^{P+L} S'\left[(K+j)T\right] n(jT) \quad (4)$$

Changing the order of summations

$$\varphi_{S'r}(KT) = \sum_{i=0}^{L} \sum_{\lambda=-i}^{P+L-i} S'\left[((K+i)+\lambda)T\right] S(\lambda T) h(iT) + \sum_{j=0}^{P+L} S'\left[(K+j)T\right] n(jT) \quad (5)$$

$$\varphi_{S'r}(KT) = \sum_{i=0}^{L} \varphi_{S'S}\left[(K+i)T\right] h(iT) + \varphi_{S'n}(KT) \quad (6)$$

where $\varphi_{S'S}(KT)$ is the cross correlation of transmitted signal S(KT) and function S'(KT).

h(iT) is the discrete impulse response.

$\varphi_{S;r}(KT)$ is the cross correlation of the function S'(KT) and any system noise n(KT) which may be present, including speech.

$$\varphi_{S'r}(KT) = \sum_{i=0}^{L} \varphi_{S'S}\left[(K+i)T\right] h(iT) + \varphi_{S'n}(KT) \quad (7)$$

Substituting $-m = K$

$$\varphi_{S'r}(-mT) = \sum_{i=0}^{L} \varphi_{S'S}\left[(-m+i)T\right] h(iT) + \varphi_{S'n}(-mT) \quad (8)$$

As h(mT) is known to exist only for $0 \leq m \leq L$, then $\varphi_{S'r}(-mT)$ is only of interest over the range $0 \leq m \leq L$ if $\varphi_{S'r}(-mT) = \gamma h(mT)$ and for $\varphi_{S'r}(-mT) = \gamma h(mT)$; then

$$\varphi_{S'r}(-mT) = \sum_{i=0}^{L} \varphi_{S'S}\left[(-m+i)T\right] h(iT) + \left[\varphi_{S'S}(0T) h(mT)\right] + \varphi_{S'n}(-mT) \quad (9)$$

since $\varphi_{S'S}(0T)$ will always occur in the range $0 \leq i \leq L$ for any $0 \leq m \leq L$.

Two other terms must equal zero; i.e.

$$\sum_{i=0}^{L} \varphi_{S'S}\left[(-m+i)T\right] h(iT) = 0, \text{ and}$$

$$\varphi_{S'n}(-mT) = 0$$

As h(iT) is known to exist (i.e., $h(iT) \neq 0$) for $0 \leq i \leq L$, then $\psi_{S'S}[(-m+i)T]$ must be zero for $0 \leq i \leq L$ and $i \neq m$, over the range $0 \leq m \leq L$.

Therefore,

$$\psi_{S'S}[(-m+i)T]$$

must be zero for $(-L+0) \leq (-m+i) \leq (L-0)$ and $i \neq m$. Also,

$$\psi_{S'S}(KT) = 0 \text{ for } -L \leq K \leq +L \text{ and } K \neq 0. \quad \text{However,}$$

$$\psi_{S'S}(KT) = \sum_{i=0}^{P} S'[(K+i)T]S(iT)$$

as S(iT) is non zero only for $0 \leq i \leq P$. For $\psi_{S'S}(KT)$ to be zero for $K \neq 0$ when S(iT) is a PRN sequence, then

$$S'[(K+i)T]$$

must be a shifted version of S(iT) for $K \neq 0$, and $S'[(K+i)T]$ must equal S(iT) for $K = 0$.

CHARACTERISTICS OF SEQUENCES

Suppose we take a Pseudorandom Binary Sequence Generator, bandpass filter it to match the channel characteristics, as shown in figure 10. We can correlate the filtered sequence with the original (extended) sequence to obtain the impulse response of the channel, as in figure 9. Fourier transforming the impulse response gives us the frequency response of the channel and/or filter.

The bilevel sequence shown in figure 9 transforms into a frequency response which droops at the higher frequency end. In fact, this droop is predictable as a sinc function which reaches 0 at 8 KHz, our clock rate, and is down approximately 2.75 db at 3400 Hz. This characteristic is shown in figure 11(a).

Figure 11(b) shows the result of using a tri-level sequence in a return-to-zero mode, where a 5 microsecond pulse of positive or negative polarity is generated at each clock interval. In this case the frequency response is essentially flat across the bandwidth.

That is, a return to zero pulse of length γ approaches a Dirac impulse function as γ approaches zero, thus preventing any frequency droop. The same thing can be accomplished by increasing the sampling rate, but this also increases the computation rate. The average power transmitted in the channel is the same in each case, since the sequence is filtered in bandwidth and adjusted in average power amplitude.

CODING CHARACTERISTICS AND PREDICTED PERFORMANCE:

Voice samples are obtained to 12 bit accuracy, but these are immediately converted to logarithmic format to only 8 bits accuracy. By using a logarithmic format, advantages of companding of the voice signal are obtained, and the correlation computations are simplified. We have predicted that quantization noise will be suppressed to greater than -36 db, and echo cancellation should also be to about that level.

OPERATIONAL CHARACTERISTICS:

Our echo canceller operates by switching between "calibrate" and "operate" modes. A single echo canceller serves 32 channels by time multiplexing, and a microprocessor is planned for programming the operation and mode switching. Generally speaking, the operational mode goes something like the following:

1. When the line connection is established, a single PRN sequence of length 1023 (about 100 milliseconds duration) is transmitted along the channel. The impulse response is calculated from correlation of the echo with the transmitted sequence. These constants are then stored in the transversal filter for echo cancellation, and the channel is switched to "operate".
2. The system remains in "operate" mode until such time as a single-point correlator indicates that echo cancellation is no longer effective.
3. On command, the system switches back to "calibrate" followed by reversion to "operate". Regular polling of all 32 channels is done by the microprocessor.

To the subscriber the PRN calibration burst sounds like a subdued hiss, and it does not significantly reduce voice intelligibility even if it is transmitted in the middle of a conversation. Even more

importantly, active speech does not interfere significantly with the accuracy of the impulse response constants obtained from the PRN burst.

Bench tests of this system are nearing completion, and we expect to start field testing shortly. Field tests will include satellite testing from our own satellite terminal at Walkworth, north of Auckland.

ACKNOWLEDGEMENT:

The authors are especially grateful to Mr. Rob B. Wilkinson, Division Engineer (Transmission), New Zealand Post Office, Wellington, for his able assistance and encouragement.

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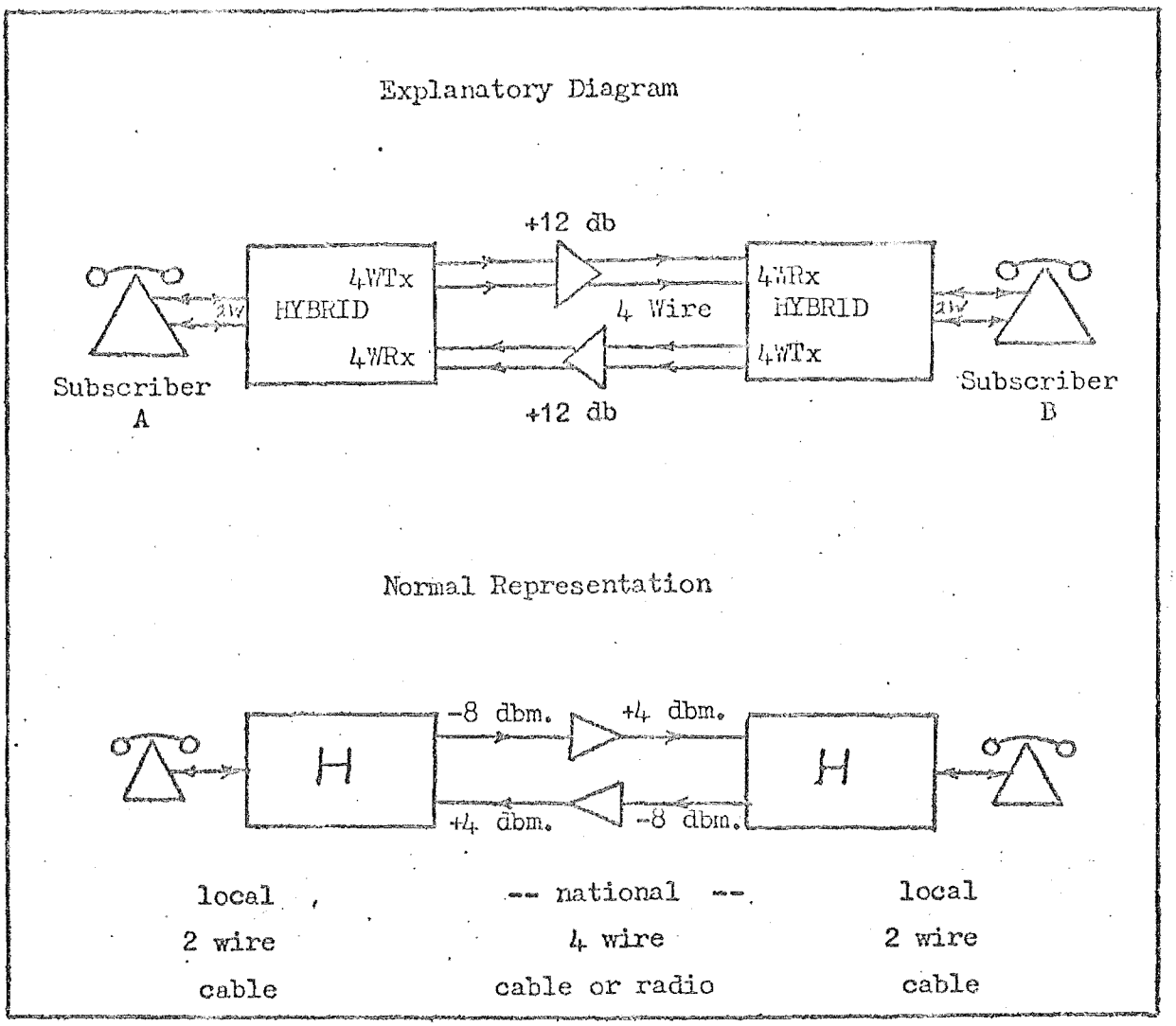


Figure 1: Block diagram of the local/national telephone network.

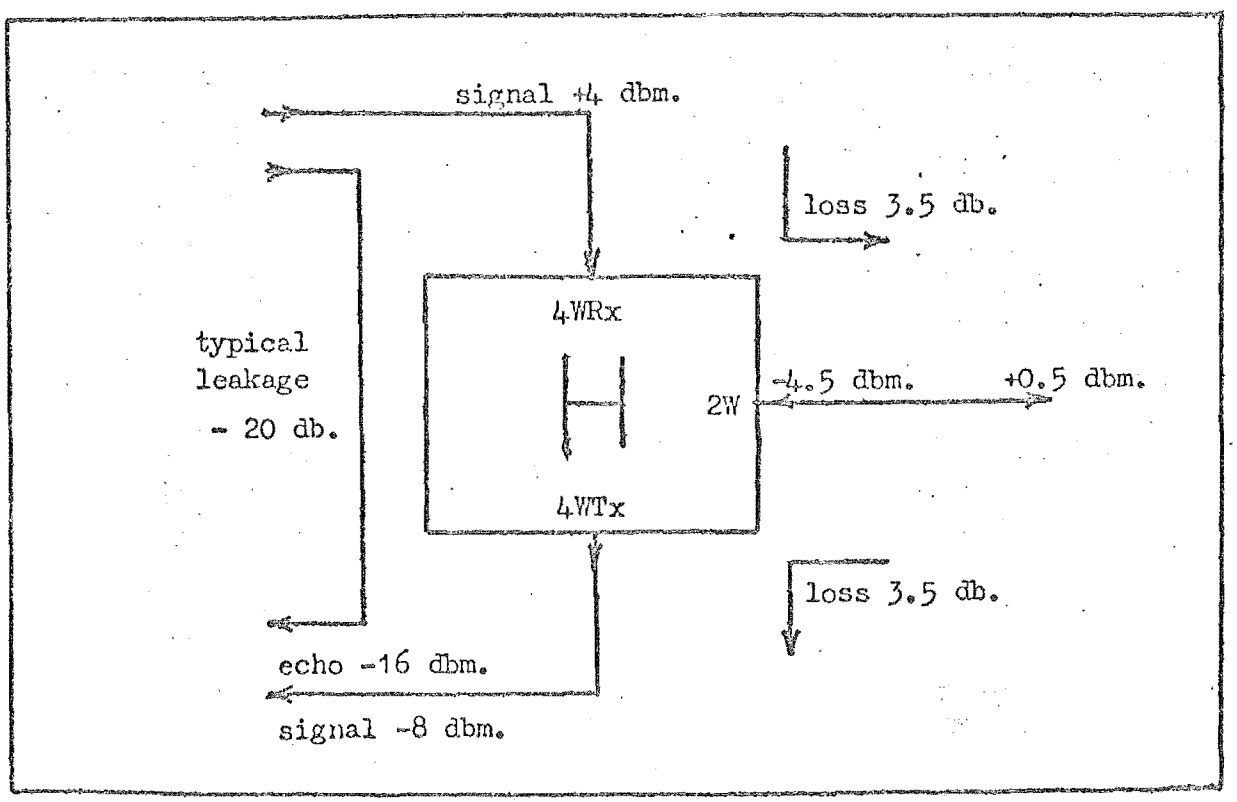


Figure 2: Typical hybrid signal levels and interconnections.

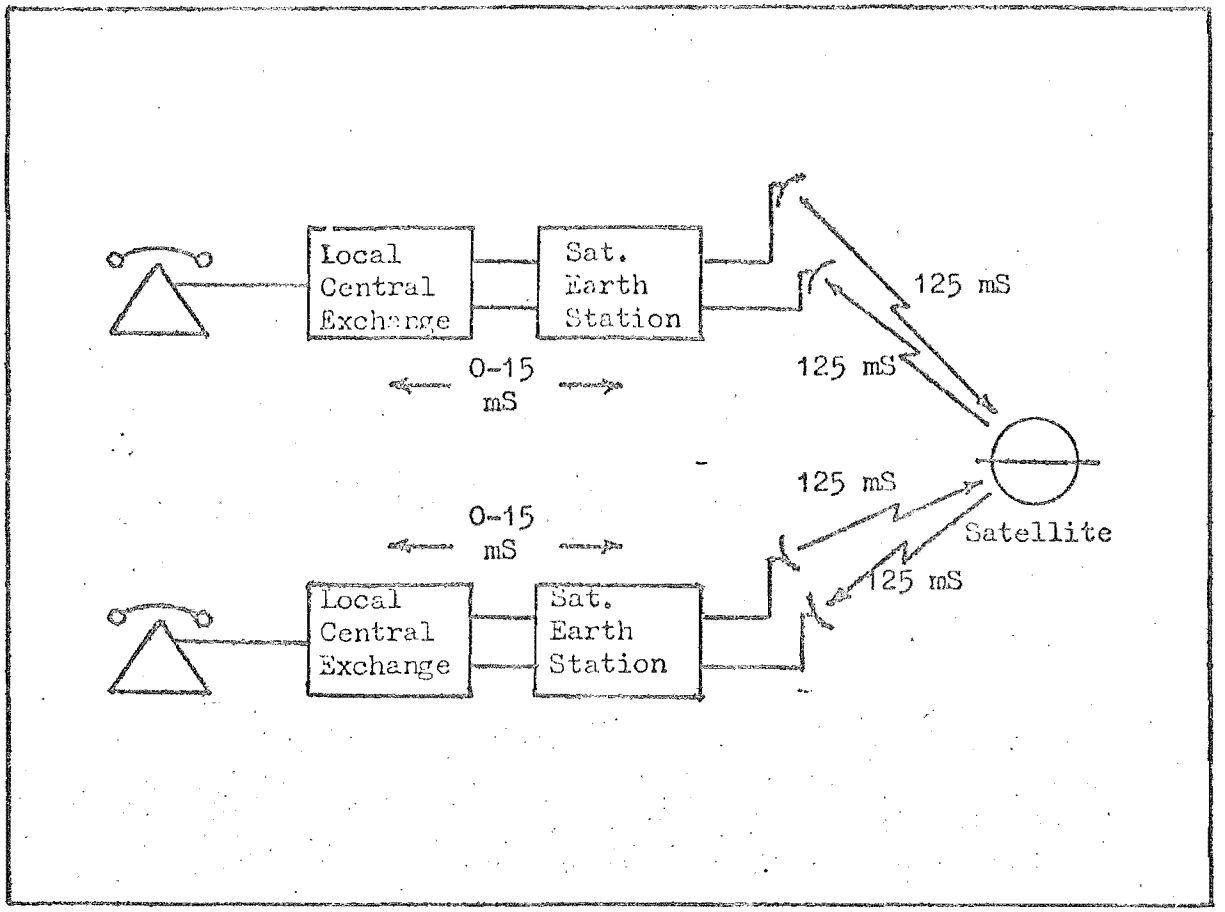


Figure 3: Satellite linked telephone circuit.

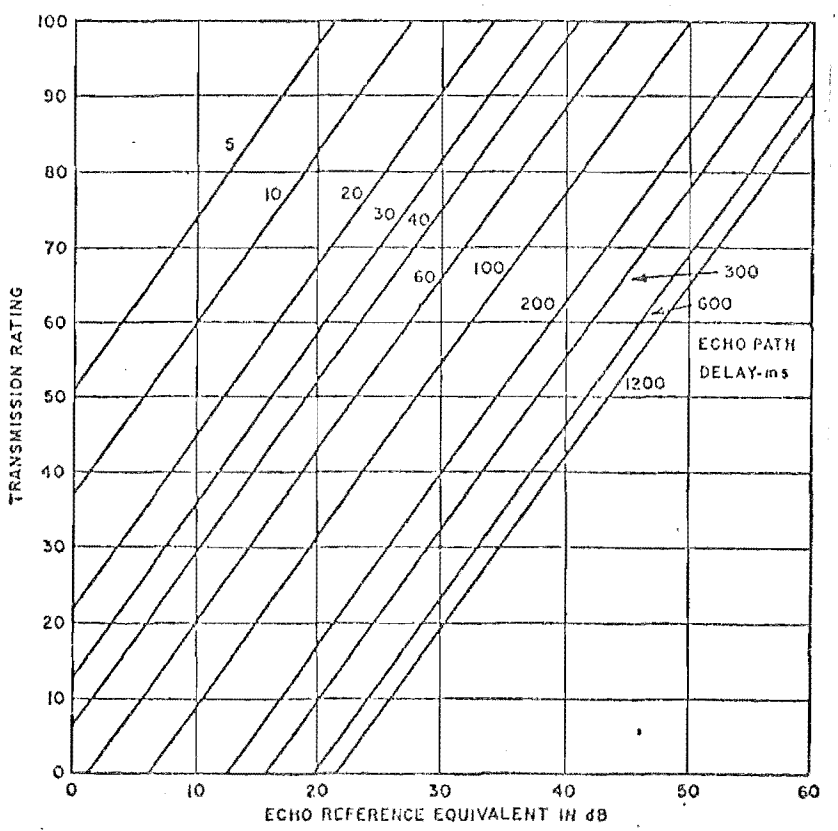


Figure 4: Transmission rating vs delay in the telephone network. (From CCITT G.529).

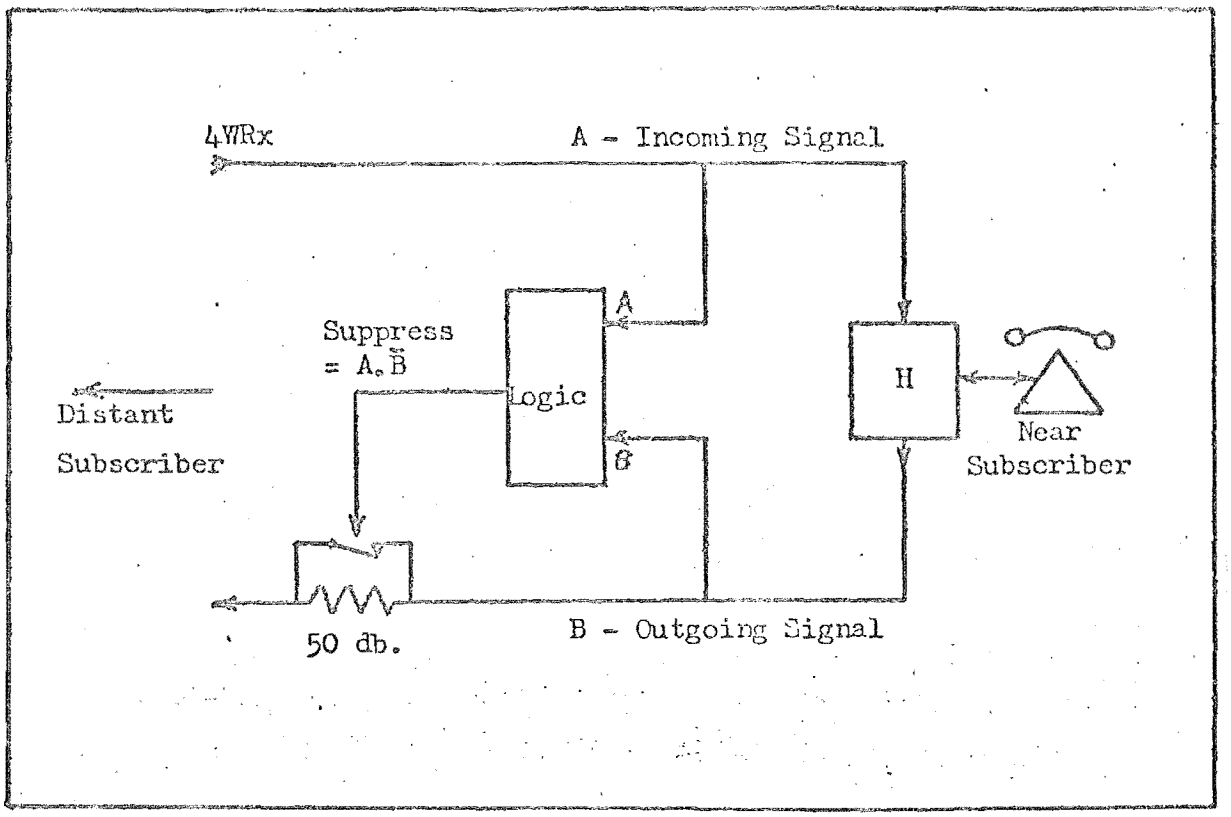


Figure 5: Echo Suppressor operation in the 4-wire network.

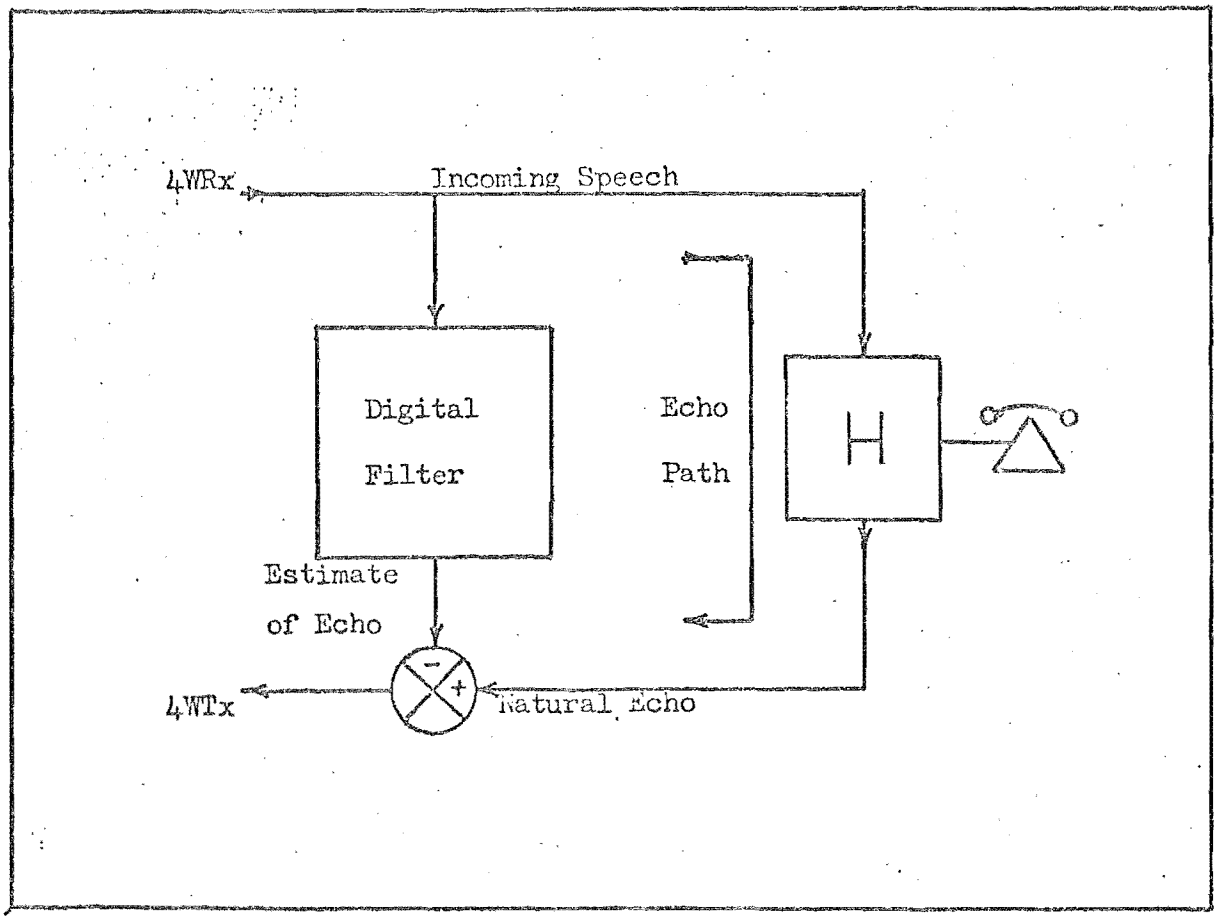
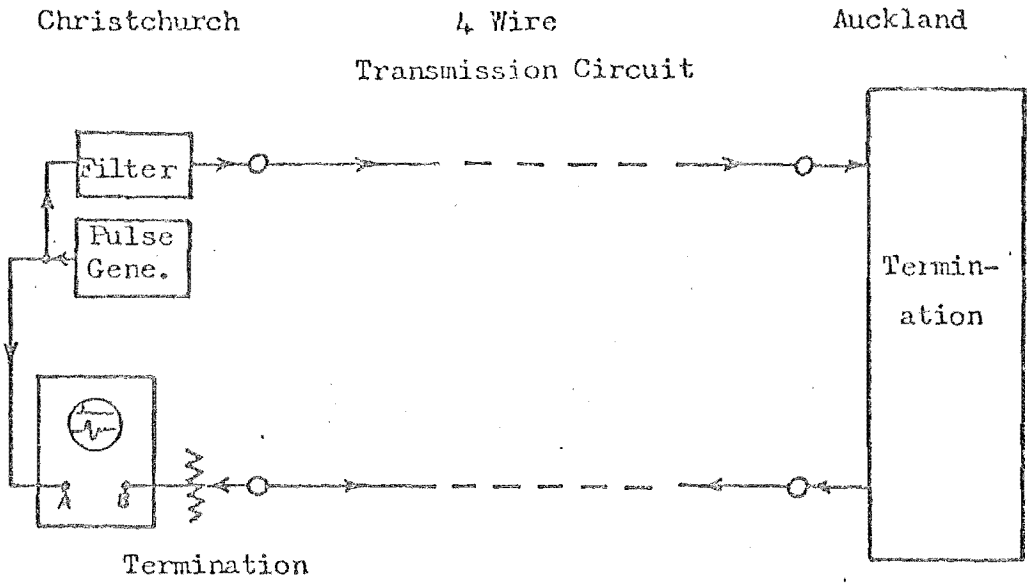
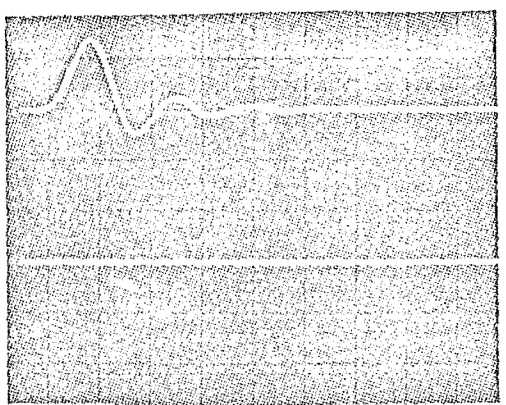


Figure 6: Echo Canceller operation in the 4-wire network.

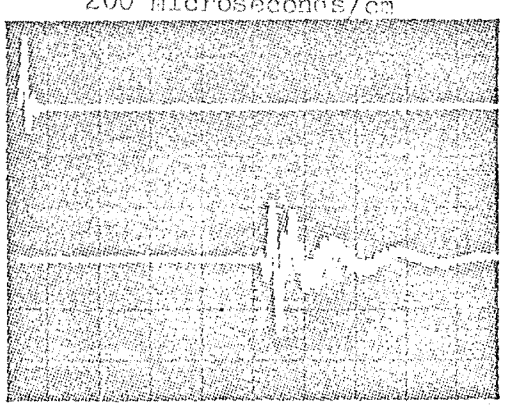


(a) Christchurch - Auckland telephone test circuit.

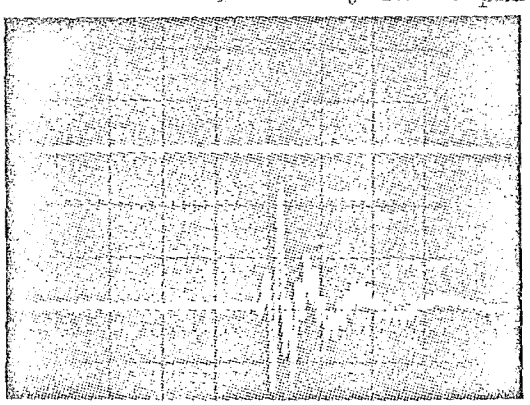


(b) Filtered impulse function
200 microseconds/cm

(c) Hybrid replaced by 12 db pad



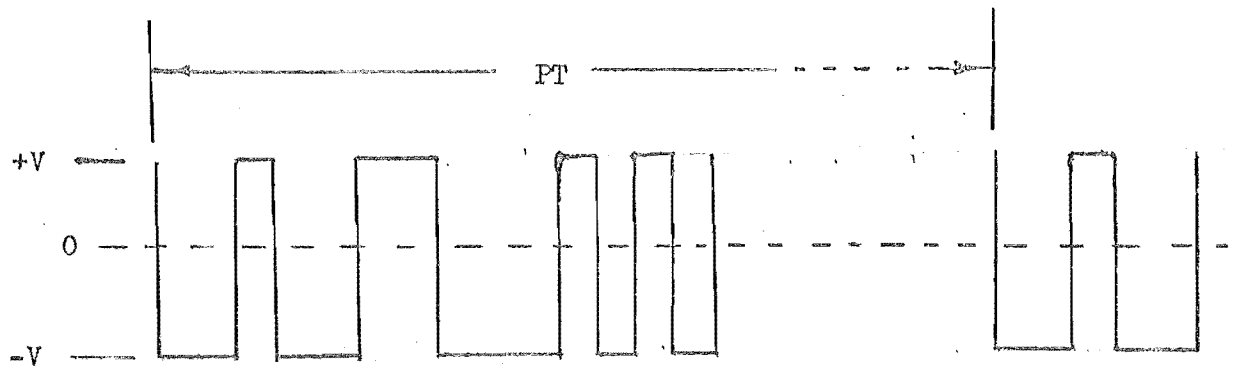
(d) Telephone termination



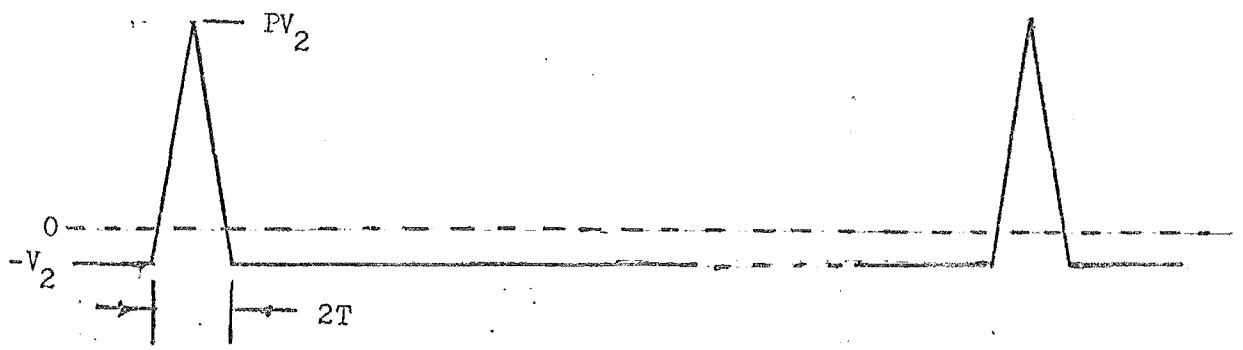
(e) 12 mile open cable termination.

Note: All but (b) are 2 milliseconds/cm time scale.

Figure 7: Tests on the New Zealand telephone 4-wire system.



(a) Pseudorandom Binary Sequence



(b) Autocorrelation function of (a) above

Fig. 8: Pseudorandom Binary Sequence and its Autocorrelation Function

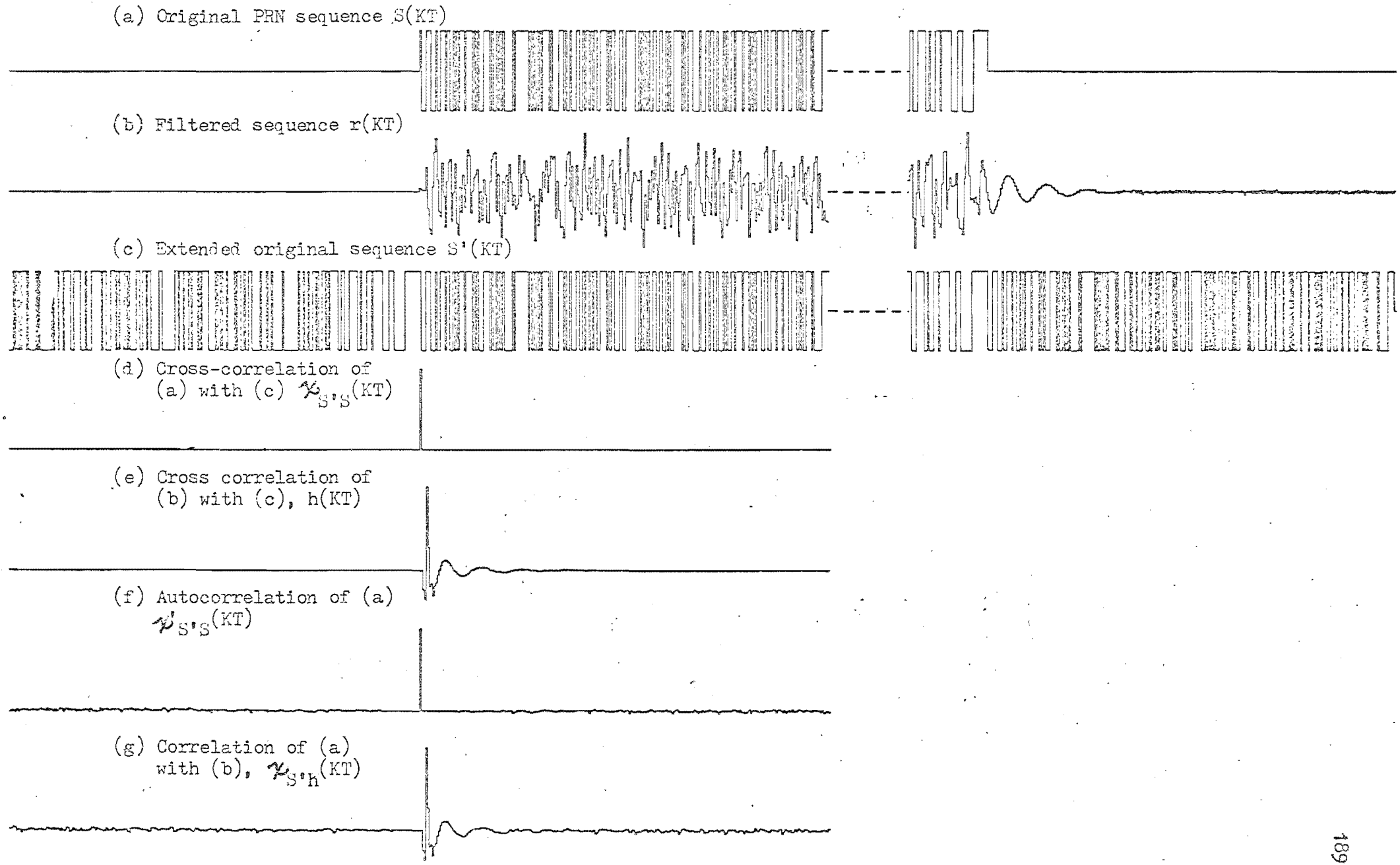


Figure 9: Characteristic waveforms obtained from a pseudorandom binary sequence of length 1023 bits.

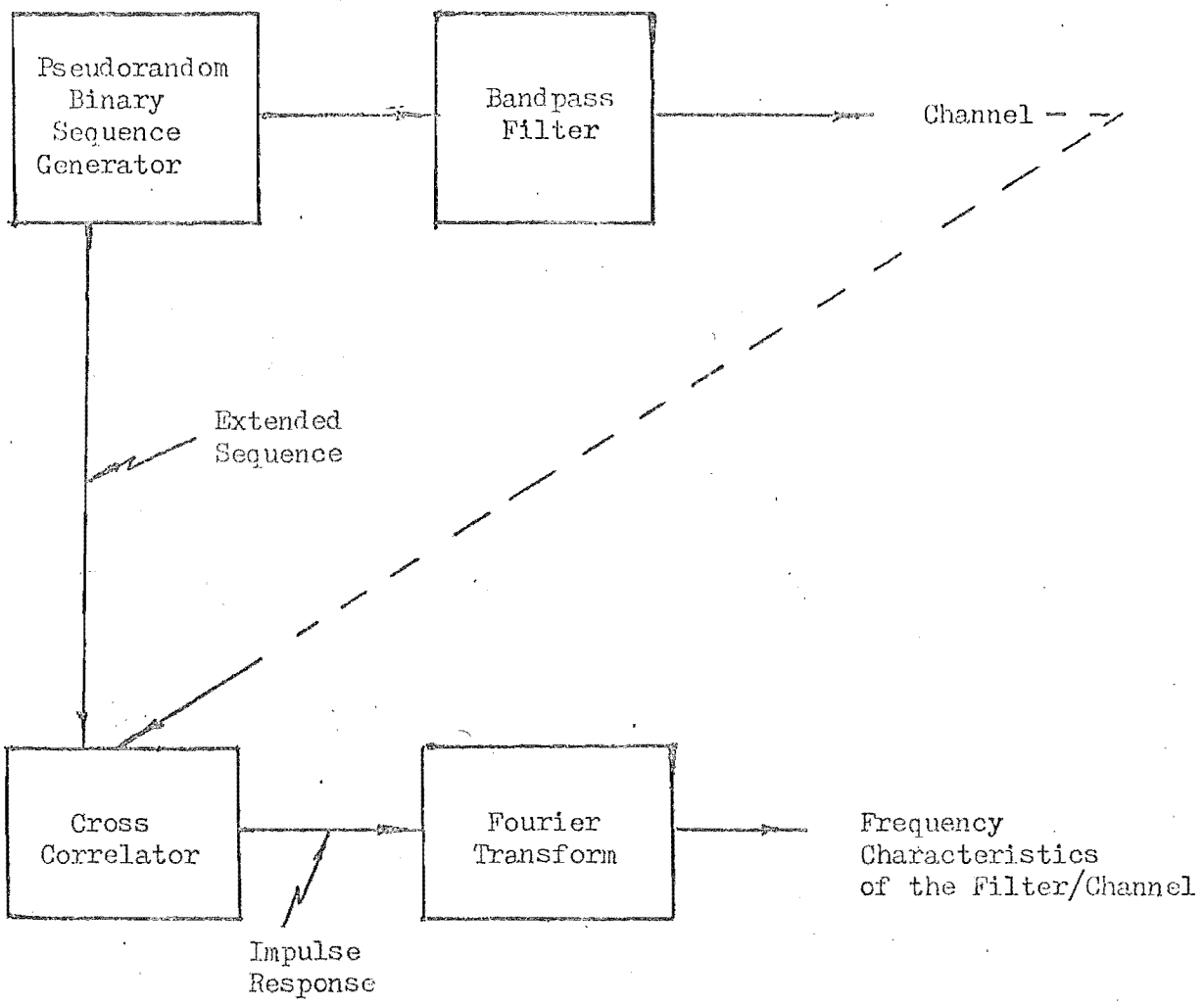
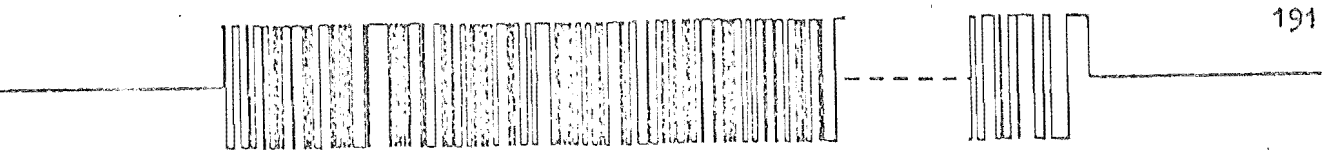
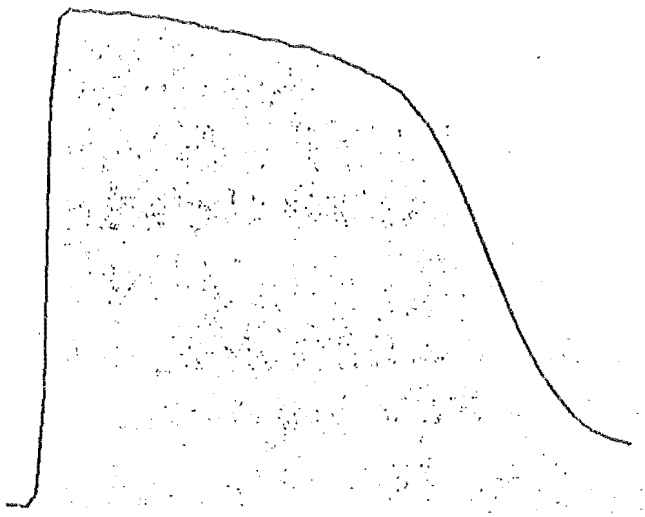
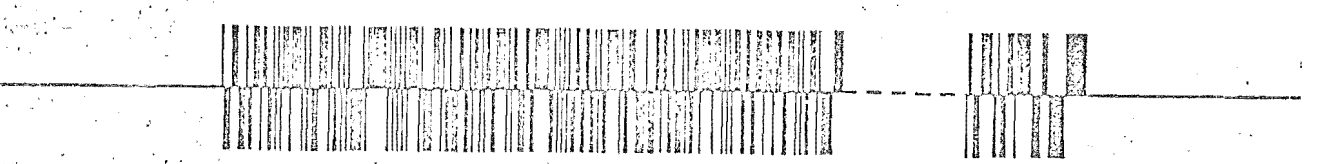


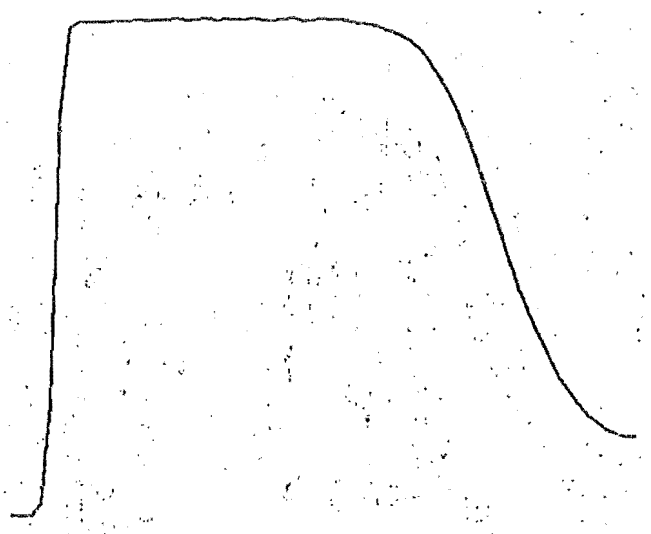
Figure 10: Measurement of the Impulse/Frequency response of a filter and/or channel.





(a) Bilevel sequence and its frequency response.





(b) Trilevel sequence and its frequency response.

Figure 11: Two Pseudorandom Binary Sequences and their frequency responses.

PRACTICAL SAMPLING CONSIDERATIONS

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Department of Electrical Engineering
University of Canterbury
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ABSTRACT

Sampling of a low pass analog signal of bandwidth B is very simple. Usually the signal is sampled and held at discrete levels, while the analog-to-digital converter is converting the sampled signal into binary numbers. Minimum clock rate is 2B. Sampling of a bandpass signal however, where the bandwidth may be a small fraction of the center frequency, can be considerably more complex. Previous publications have shown minimum sampling rates for bandpass signals, but even when these criteria are met, aliasing can still occur. This paper demonstrates that such aliasing "bands" exist in all cases where sampling is reduced below twice the highest signal frequency f_h.

DISCUSSION

GENERAL

Figure 1 shows a simple sampling process. A sample-and-hold circuit samples the input signal at discrete levels and holds these values until the analog-to-digital converter converts the level into binary bits. Clock sampling frequency f_s synchronizes sample-and-hold circuit and analog-to-digital converter. If the signal is to be converted into N binary bits, to prevent errors greater than $\pm \frac{1}{2}$ bit, the aperture time (aperture jitter) Δt must be kept to less than the following:

$$\Delta t \leq 1/2^N W_h \qquad (1)$$

where $W_h = 2\pi f_h$

Minimum sampling rate is 2B, and for a low-pass system, this means $2f_h$, where f_h is the highest frequency in the bandwidth.

SAMPLING OF BANDPASS SIGNALS

To see what happens in the case of a bandpass signal, consider B to be fixed, as f_h is increased, as shown in figure 2. The sampling rate must be increased with increasing f_h until it reaches 4B at the point where $f_h = 2B$. Now it is evident that the sampling rate can be dropped from 4B to 2B without aliasing, since the aliasing frequency will fall between 0 and B.

But all of the foregoing principles have been published previously in the literature.[1-7] Figure 2 is widely publicized as the aliasing characteristics of a bandpass signal. Our own investigations show that figure 2 gives a totally inaccurate picture of bandpass sampling, which can lead to aliasing at sample rates well above these minimum values. In fact, aliasing can occur any time the sample rate is dropped below $2f_h$, which means that it can occur in any case of bandpass sampling as opposed to simple lowpass sampling.

Figure 3 is a revised graph of the bandpass sampling function. Shaded areas of this graph are the permissible sampling regions, with the white bands being aliasing regions. The validity of this graph can

be tested very simply and interestingly by sampling a narrow bandwidth signal at rate $2f_h$, then dropping the clock rate and observing the aliasing bands.

VECTOR SAMPLING

In the case of vector sampling, two quadrature components of the signal vector are sampled simultaneously. Minimum sample rate for vector sampling is always $f_s = B$ sample PAIRS. The same number of samples are handled in this case, but since they are handled in 2 parallel channels, the clock rate is reduced by 2:1. Figure 4 shows 2 examples of vector sampling; one using the Hilbert Transform, and the other using a quadrature local oscillator to generate a Hilbert Pair.[8]

The vector time function G(t) can be expressed in terms of its Hilbert Pair components as follows:

$$G^2(t) = g^2(t) + \hat{g}^2(t) \qquad (2)$$

where $\hat{g}(t)$ is the Hilbert Transform of $g(t)$, as shown in figure 4.

The component $g(t)$ is the real component of the vector, and an even ordered function. Component $\hat{g}(t)$ on the other hand is the imaginary component of the vector, and an odd ordered function. The distinction is that even ordered functions are characterized by

$$g(t) = g(-t) \qquad (3)$$

$$\hat{g}(t) = -\hat{g}(-t)$$

Figure 5 shows a graph of a typical even ordered function and its equivalent odd ordered function. Since the Hilbert Pair completely define the characteristics of the vector, there is no aliasing of the sample function as long as $f_s \geq B$.

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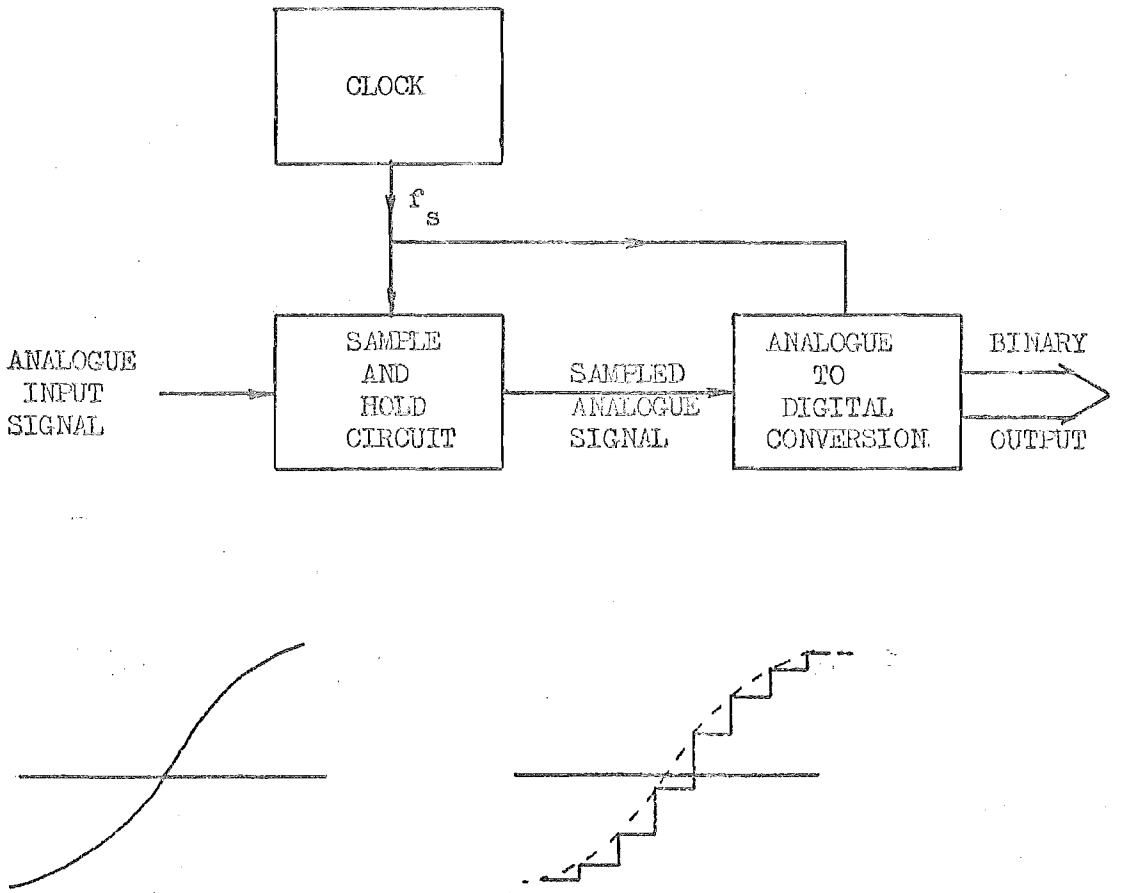


Fig. 1. Simple sampling circuit.

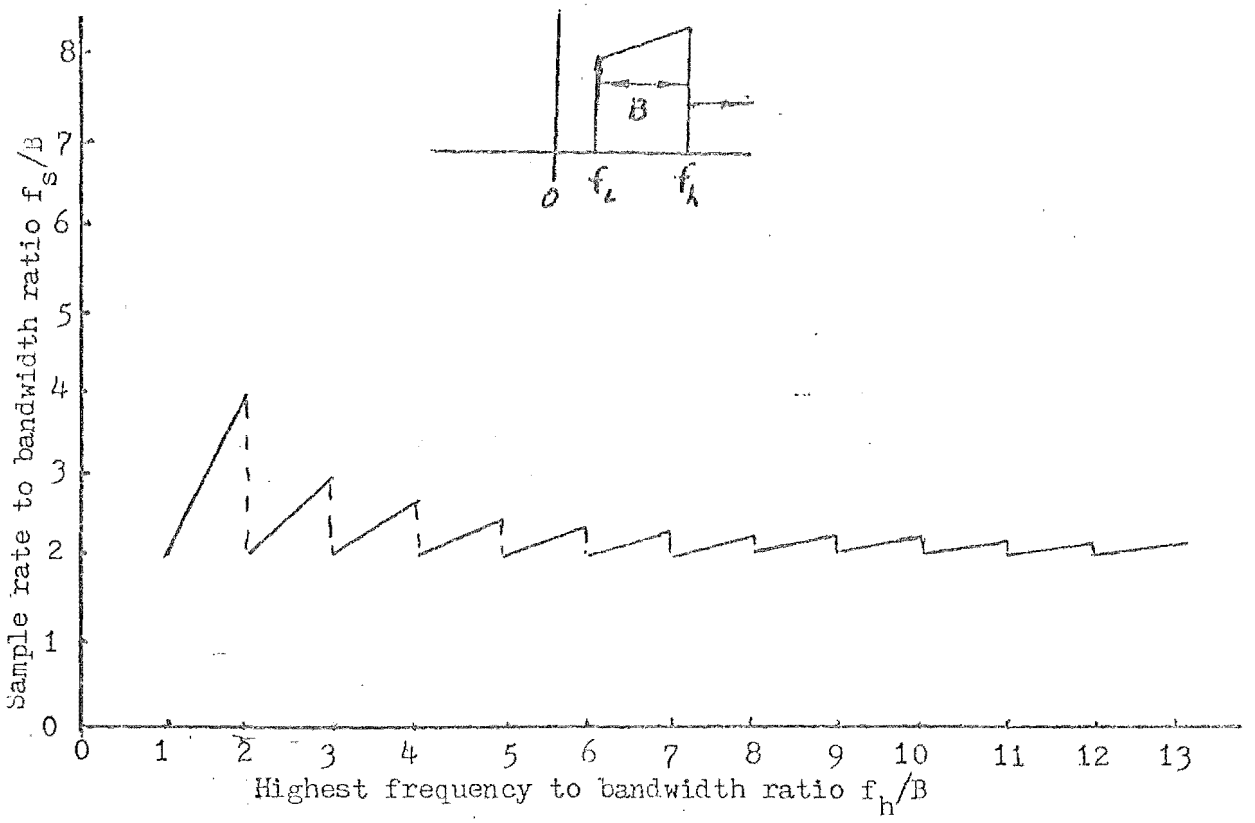


Figure 2: Minimum sample rate for a bandpass signal, from literature.

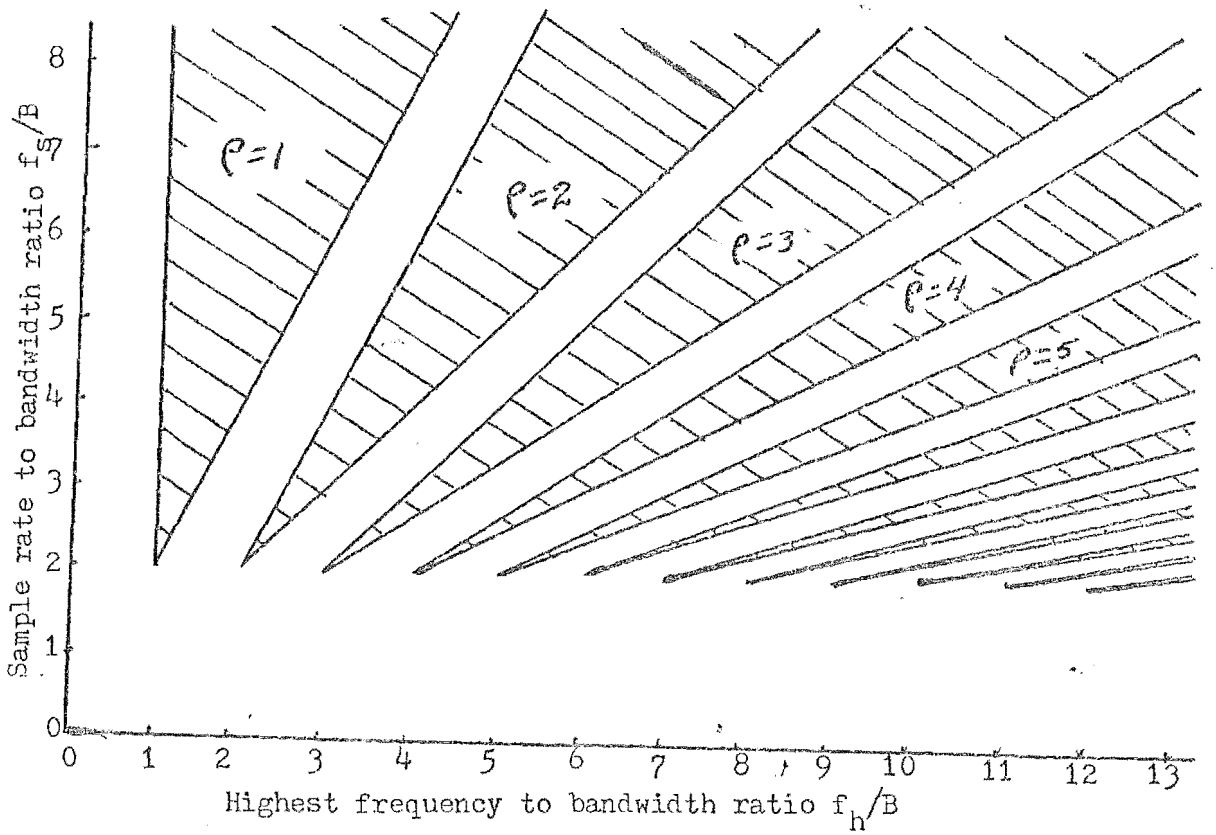
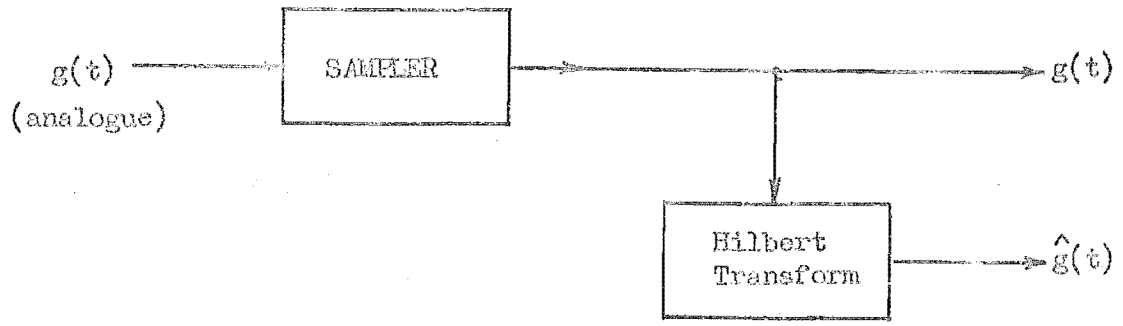
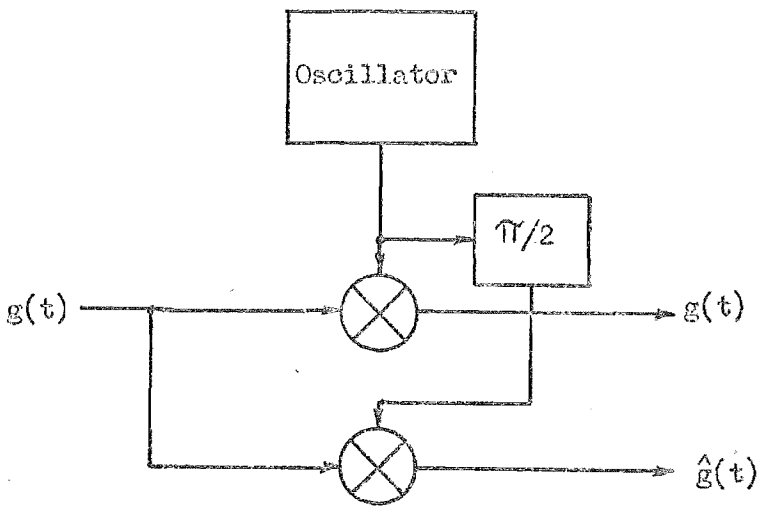


Figure 3: Sample rate for a bandpass signal, by exact analysis.

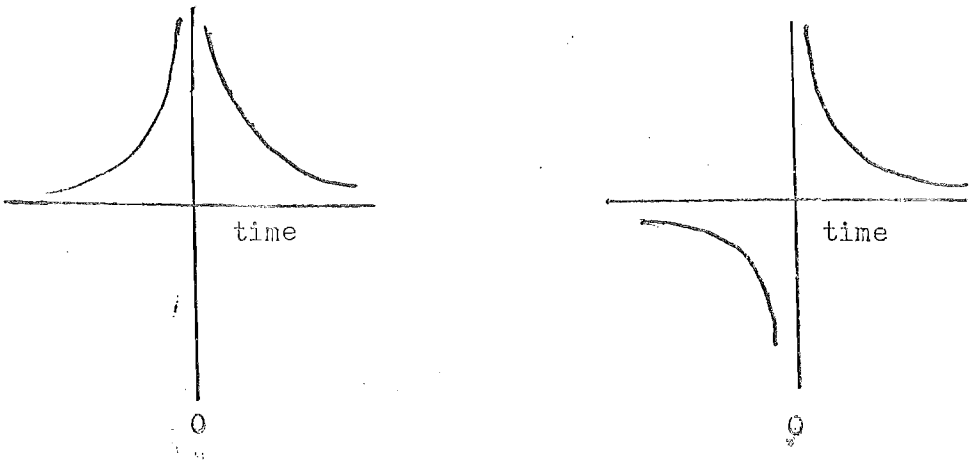


(a) Generating a Hilbert Pair by transformation



(b) Generating a Hilbert Pair by quadrature local oscillator

Fig. 4. Two methods for generating a Hilbert Pair for representing the signal vector



(a) Even ordered function $g(t)$

(b) Odd ordered function $\hat{g}(t)$

Figure 5: An example of a typical even ordered function and its equivalent odd ordered function. (from Haykin).

APPENDIX II

THE CONVOLUTION THEOREM

$$h(t) * x(t) \Leftrightarrow H(f) \cdot X(f)$$

Where $\Leftrightarrow$ denotes the fourier transform and H(f) and X(f) are the fourier transforms of h(t) and x(t) respectively.

PROOF:

now; $$X(f) = \int_{-\infty}^{\infty} x(t)\ e^{-j2\Pi ft} dt$$

and $$x(t) = \int_{-\infty}^{\infty} S(f)\ e^{\ j2\Pi ft} df$$

By transforming both sides of the convolution equation;

$$y(t) = \int_{-\infty}^{\infty} x(\tau) \cdot h(t - \tau)\ d\tau$$

the resulting expression is

$$Y(f) = \int_{-\infty}^{\infty} y(t)\ e^{-j2\Pi ft} dt$$

$$= \int_{-\infty}^{\infty} \{ \int_{-\infty}^{\infty} x(\tau) \cdot h(t - \tau)\ d\tau \}\ e^{-j2\Pi ft} dt$$

and changing the order of integration

$$Y(f) = \int_{-\infty}^{\infty} x(\tau)\{\int_{-\infty}^{\infty} h(t-\tau)\ e^{-j2\Pi ft}dt\}\ d\tau$$

Now let $\gamma = (t - \tau)$ then

$$\{\int_{-\infty}^{\infty} h(t-\tau)\ e^{-j2\Pi ft}dt\} = \int_{-\infty}^{\infty} h(\gamma)\ e^{-j2\Pi f(\gamma+\tau)}\ d\gamma$$

$$= e^{-j2\Pi f\tau}\int_{-\infty}^{\infty} h(\gamma)\ e^{-j2\Pi f}\ d\gamma$$

$$= e^{-j2\Pi f\tau}.H(f)$$

Therefore;

$$Y(f) = \int_{\infty}^{\infty} x(\tau)\ e^{-j2\Pi f\tau}.\ H(f)\ d\tau = H(f)\ .\ X(f)$$

This shows the equivalence of multiplication in the frequency domain with convolution in the time domain.

APPENDIX III

THE EFFECT OF A SAMPLE AND HOLD CIRCUIT

The best method of determining the effect of the sample and hold circuit is to construct the sample and held waveform in stages and analyse the effect of each subsequent stage. This will be done in Fig. A3.1.

The function f(t) is first sampled by the function s(t) resulting in; $f'(t) = f(t) \cdot s(t)$. The resultant function will contain the original information contained in f(t) as well as upper and lower sidebands of the harmonics of s(t). The assumption is made that the sampling rate is greater than twice the highest frequency present in f(t).

To obtain the held waveform from this sampled waveform f'(t) it is convolved with the rectangular function r(t). The sampled and held waveform is therefore;

$$f_{sh}(t) = \int_{-\infty}^{\infty} f'(t) \cdot r(t - \tau)\, d\tau$$

Now convolution in the time domain is equivalent to multiplication in the frequency domain. When it is considered that the function r(t) has a (sin x)/x amplitude characteristic in the frequency domain it will be realised that it acts as a crude form of low pass filter. As the first zero of the amplitude response is at a frequency $1/\tau$

this filter will provide attenuation of around 3 dB at 3.5 KHz which is of vital importance if speech is being cancelled with components up to this frequency.

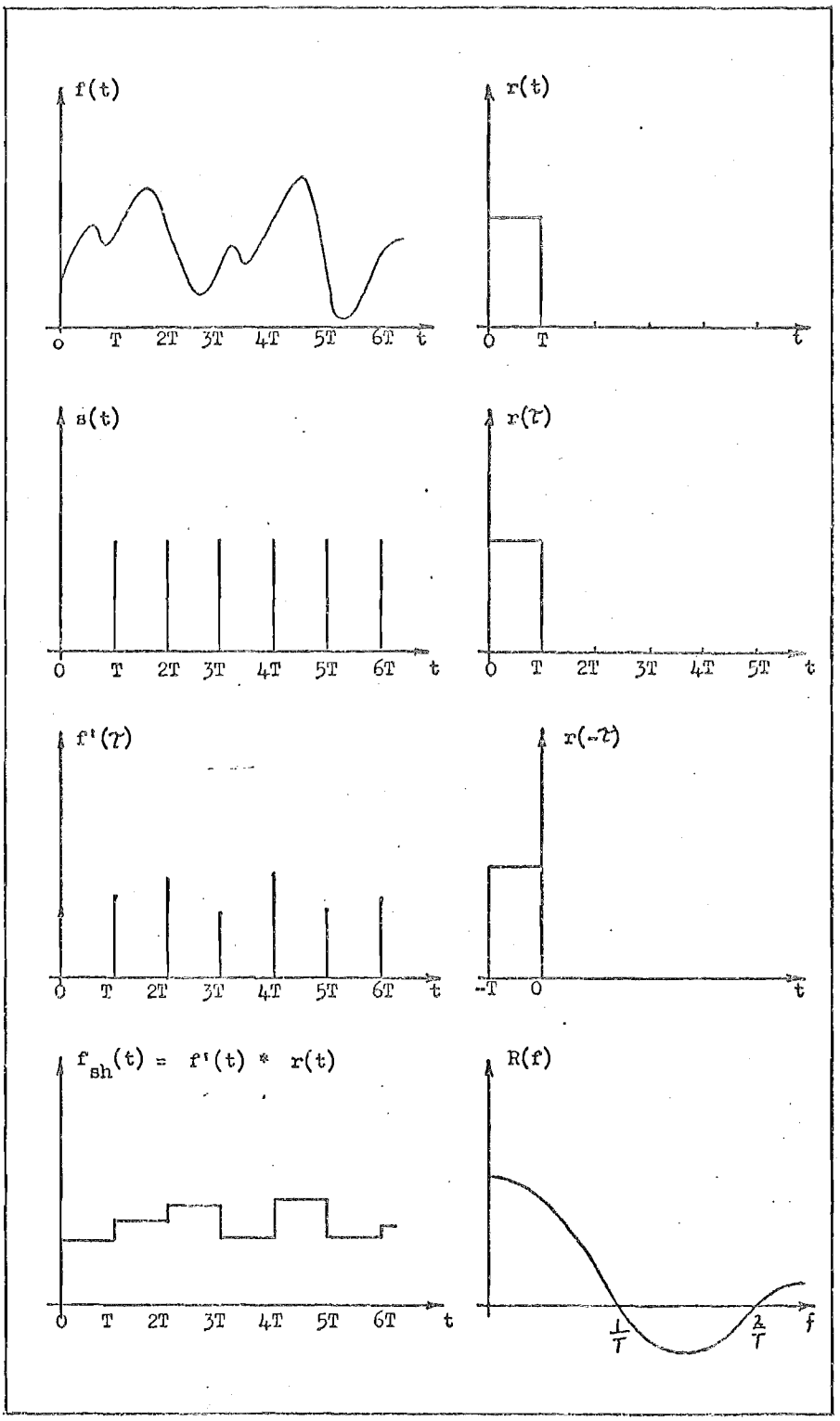


Fig. A3.1. Construction of the Sample and Hold waveform

APPENDIX IV

PART 1

5 BIT ECHO CANCELLER CIRCUITRY AND CONSTRUCTION

The echo canceller is constructed on five standard D.I.P. plug-in circuit boards enabling easy access to components by using an extension board. All digital logic is standard T.T.L. with memory and interfacing circuitry being T.T.L. compatible. All integrated circuits are easily replaced, being mounted on plug-in sockets of the dual in line type.

The prototype echo canceller is conveniently distributed on the five circuit boards in a manner illustrated in Fig. A4.1. The boards are given the following self-explanatory titles;

(1) Analogue Board

(2) Interface Board

(3) Convolution Board

(4) Control Board

(5) Relative Addressing Board

A description of basic circuit operation follows with reference to block diagrams and integrated circuits numbered

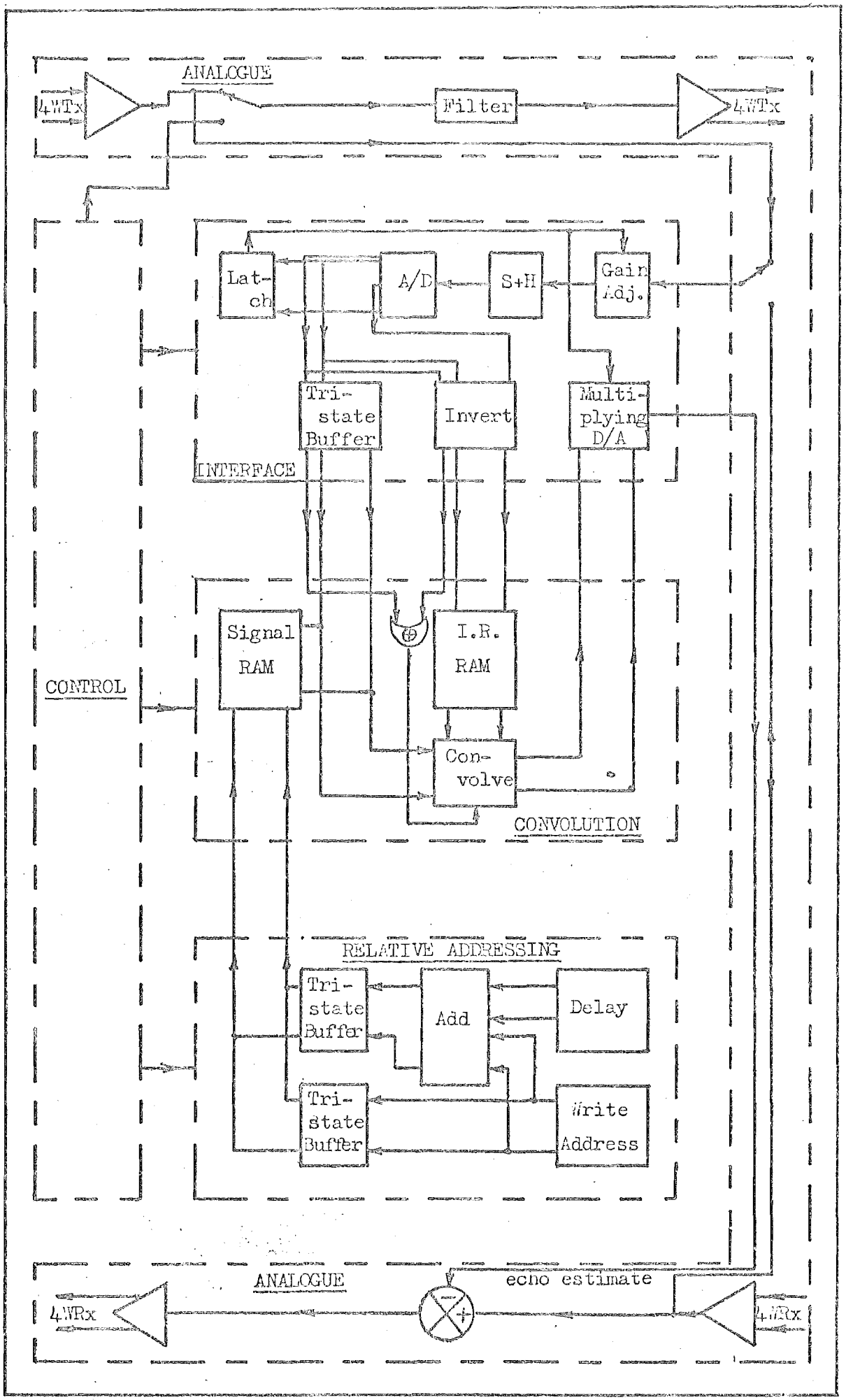


Figure A4.1 Echo canceller Circuit Board Distribution.

(3,5) in accordance with detailed circuit diagrams and descriptions later in Part 2.

I ANALOGUE BOARD

This board (see Fig. A4.2) provides for the connection to transmission circuits on which this echo canceller will be tested. A 600Ω balanced impedance match is required for the four input/output connections to the board. For signal processing on the board the signal paths are converted to an unbalanced path. This simplifies filtering and interfacing with digital circuitry. The board also provides for solid state switching for choosing the various combinations of analogue circuitry for the different phases of the calibration cycle. The following description should be followed while referring to Fig. A4.2.

The outgoing speech enters at the 4 Wire transmit input (4W TxI) terminals as a 600Ω balanced input and is immediately transformed to unbalanced signal paths with operational amplifiers (7A,7B) and either 6A or 6B. Attenuation of 16.7 dB is provided for the through signal which is routed via an analogue switch (5B), through a buffer (1A), a 3.5 KHz low pass filter (1B,2A,2B,3A) and is converted back to a 600Ω balanced impedance (3B,4A,4B). The 16.7 dB of attenuation compensates for the mid-band gain of the filter. The analogue switch (5B) provides for the transmission of calibration pulses.

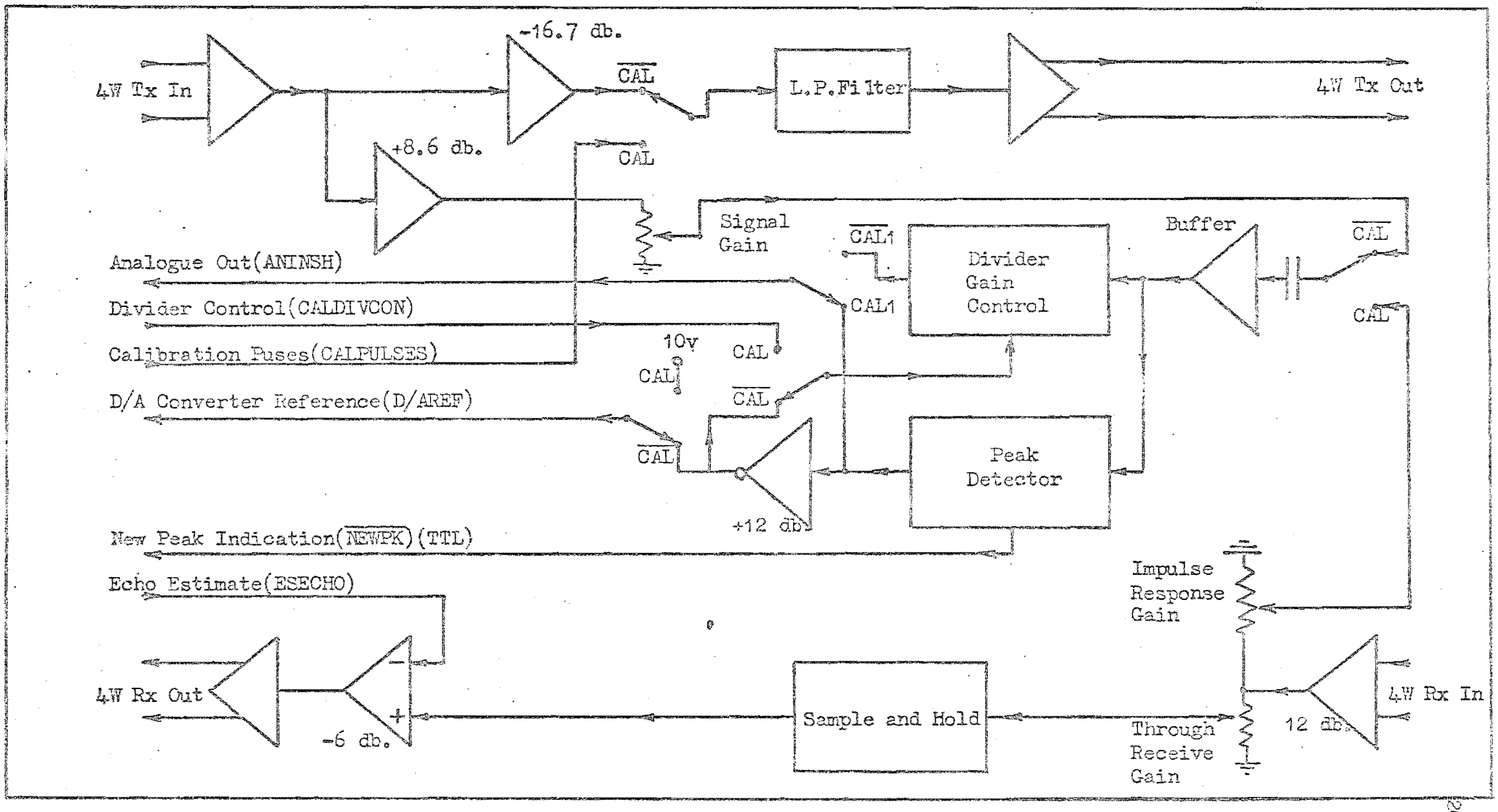


Figure A4.2 Analogue Board Block Diagram.

The return path for the echo and return speech from the near subscriber enters the 4 Wire receive input (4W RxI) port and is converted to an unbalanced path with 12 dB gain (8A,8B,11B). Gain control is provided for the through signal which is then subject to cancellation by the estimated echo (11A) and the resultant signal is converted back to a 600Ω balanced output impedance (12A,12B) at the 4 Wire receive output (4W RxO) port.

The outgoing speech to the near subscriber enters the canceller with 8.6 dB gain (6B) to bring the maximum peak expected up to 5v, to allow adjustment to 2.5v. This is then connected through an analogue switch (5A), buffer (15B), divider gain control (9,14A) and through an analogue switch (13A) out to the interface board for A/D conversion.

The impulse response from the echo path enters the canceller from the receive path (11B) through gain adjustment potentiometer, analogue switch (5A), buffer (15B), divider gain control (9,14A), analogue switch (13A) and out to the interface board for A/D conversion.

Control of the divider gain adjustment (9,14A) is governed by either the analogue peak voltage (16A,16B) with + 12 dB of gain (15A) during normal operation or by a control voltage (CALDIVCON) derived from the interface board. This voltage is the stored version of the peak value of the unscaled impulse response obtained by the interface board via analogue switch (13A) and peak detector (16A, 16B) during the first phase of the calibration cycle (CAL.CAL1).

It returns to the analogue board to control the divider during the second half of the calibration cycle (CAL.$\overline{\text{CAL1}}$) via analogue switch (10A).

The peak detector as well as providing a negative analogue voltage equal in magnitude to the peak voltage input provides an active low T.T.L. signal ($\overline{\text{NEWPK}}$). This indicates that a new peak has occurred and directs the storage of the peak amplitude and the delay to that peak during the first phase of calibration.

The analogue output 'D/AREF' provides a reference for the multiplying D/A converter on the interface board. This is a constant voltage during calibration, but under normal operation is proportional to the output of the peak detector monitoring the input signal. The theory behind the operation of this is described in Chapter 2 under signal sample scaling.

The calibration cycle consists of two separate phases, the first phase (CAL1) permits the sampling of the unscaled impulse response to determine the absolute level of the peak value of the impulse response and lasts for 60 mS. The second phase follows immediately with another calibration pulse, the response to which is scaled in amplitude. 'Normal' operation refers to the circuit operating as an echo canceller following calibration.

II INTERFACE BOARD

This board (see Fig. A4.3) interfaces the analogue circuitry to the digital circuitry. It provides for A/D

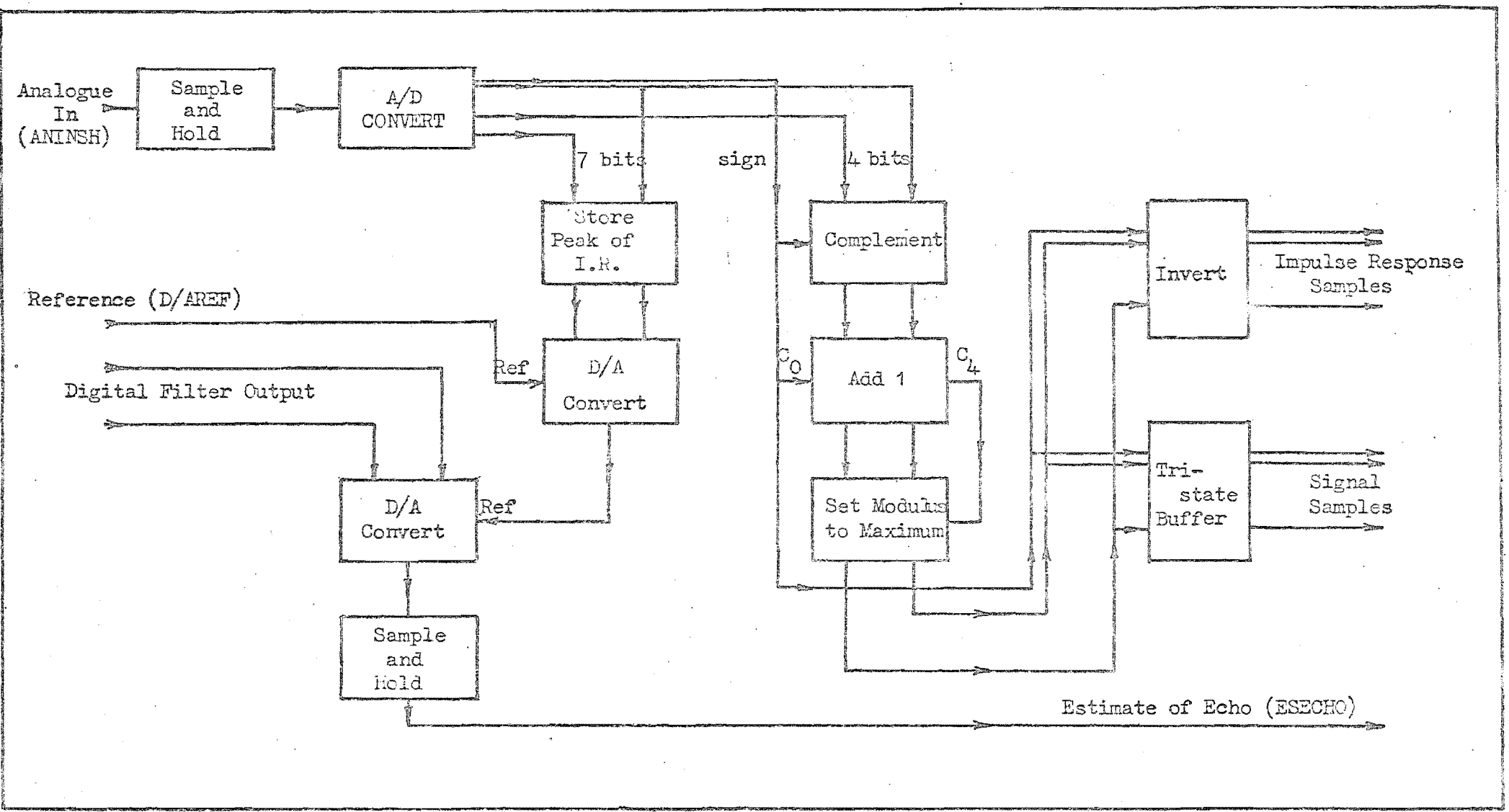


Figure A4.3 Interface Board Block Diagram

conversion with post convolution scaling and D/A conversion. It provides for the storage of the peak magnitude of the unscaled impulse response and for conversion from complementary offset to sign and magnitude digital format for samples.

The analogue input (ANINSH) is sampled and held (8) according to the control voltage (SAHDRD) and converted to complementary offset format (16) following the start conversion pulse (SCON). During normal operation and the second phase of calibration, the A/D converter is short cycled to 5 bit operation with the output being converted to sign and magnitude format (10,6,7). The 5 bit sign and magnitude output is connected to the signal RAM input/output BUS through the tri-state buffer (4) which is enabled by the active low control $\overline{\text{ENWD}}$. This output is inverted for use by the impulse response RAM during the recording of impulse response samples.

The peak value of the unscaled impulse response is stored directly as 7 bit magnitude due to the peak detector output being negative. This 7 bit latch is operated by the control signal 'STEDAP'. The output of the latch provides the digital input to the multiplying D/A converter (9) which when multiplied by the input reference, provides the reference for post convolution scaling in the second multiplying D/A converter (1). The reference for the former D/A converter (D/AREF) is proportional to the peak signal value during normal operation or a constant voltage during calibration

and is discussed at length in Section I of this chapter.

The D/A converter (1) for the digital output from the convolution board provides the scale analogue output which is the estimate of the echo value at time 'T' after the latest sample was taken. This is sampled and held (2) and passes to the analogue board to cancel the natural echo.

The analogue output CALDIVCON is the divider control voltage for the analogue board and provides for scaling the impulse response during calibration as described in the first section of this chapter.

III CONVOLUTION BOARD

This board (see Fig. A4.4) is the heart of the filter and provides for the storage of both impulse response and signal samples. The convolution process is carried out on this board including all the high frequency (1 MHz) timing for the reading of stored sample values, multiplication and accumulation. It was considered preferable to restrict this relatively high frequency section to the one circuit board.

The 0 to 63 address counter (3,4) provides the write address and read address for the impulse response RAM (14). During calibration it is incremented at an 8 KHz rate from an external clock while samples are stored. During each read cycle it is incremented from 0 to 63 at a 1 MHz rate by the 1 MHz timing on this board. A 'clear' control is externally operated and an output is provided (COUNT=64) which indicates that the read cycle, or write cycle during calibration is complete.

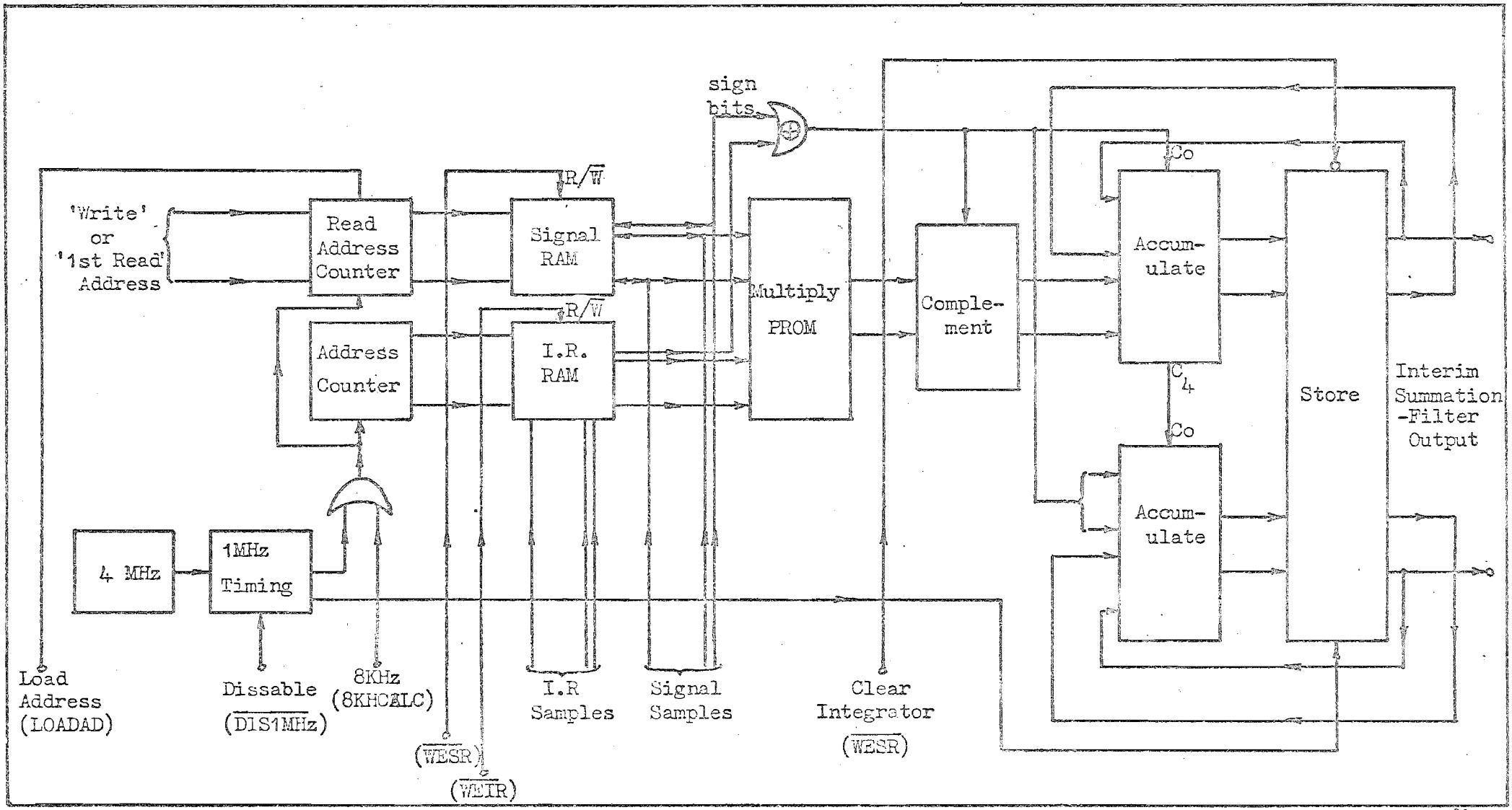


Figure A4.4 Convolution Board Block Diagram

The 0 to 255 counter (5,6) provides the address for the signal RAM (9,10). The write address is loaded into the counter from the relative addressing board every sample period at which time the signal sample is stored. Once the signal sample is stored the first read address is loaded from the relative addressing board and the read cycle commences, with the counter incrementing from the first read address simultaneously with the 0 to 62 counter for 63 increments at which point the read cycle finishes. An active low $\overline{\text{LOAD}}$ control is provided for external control.

The 1 MHz timing circuit uses an 8 MHz crystal controlled clock, a divide by 2 circuit and a shift register for generating sequential timing and effectively dividing by 4 to get 1 MHz. An 'enable' control is incorporated for external control during the write and calibration cycles.

The impulse response RAM (14) has separate input/output ports with the only control being the Read/$\overline{\text{Write}}$ control which is taken low during the calibration cycle only. The only other variable used is the address, as the RAM is permanently enabled.

The signal RAM (9,10) is also permanently enabled but has common input/output ports. Tri-state buffering is provided for the input by the interface board. In the read cycle only the address is changed and the Read/$\overline{\text{Write}}$ control taken low for the write cycle only.

The magnitude samples are applied to the address of a permanently enabled PROM (11) which provides a multiplication look-up table as its output. The product is scaled by

a factor of 240/255 to give an output of 1111 (240) for two input magnitudes of 1111 (15). The sign bits out of the RAM's are checked and the PROM's output is 2's complemented if the product should be negative. Accumulation is then achieved using 2's complement arithmetic, with the output of the adders (8,12) being clocked into a parallel load shift register (16) whose output at any time is the interim summation. This is connected back to the input of the adders for updating every time a new pair of samples is multiplied together by the PROM. At the end of the read cycle the output of the subsequent D/A converter on the interface board is sampled and held prior to the clearing of the accumulator.

IV CONTROL BOARD

This section of the filter (see Fig. A4.5) coordinates and controls the operation of the remainder of the canceller. It generates timing pulses at an 8 KHz rate and provides general logic for the system. By a combination of timing pulses generated within this board, along with incoming status signals, control signals are generated and transmitted to other boards.

The timing pulses for normal circuit operation are generated by six monostable multivibrators (1(Qa,Qb),2(Qc, Qd),10(Qe,Qf)) operating at a clock frequency of 8 KHz generated by a free running clock circuit (16). A diagram showing the timing sequences is shown in Fig. A4.6(a).

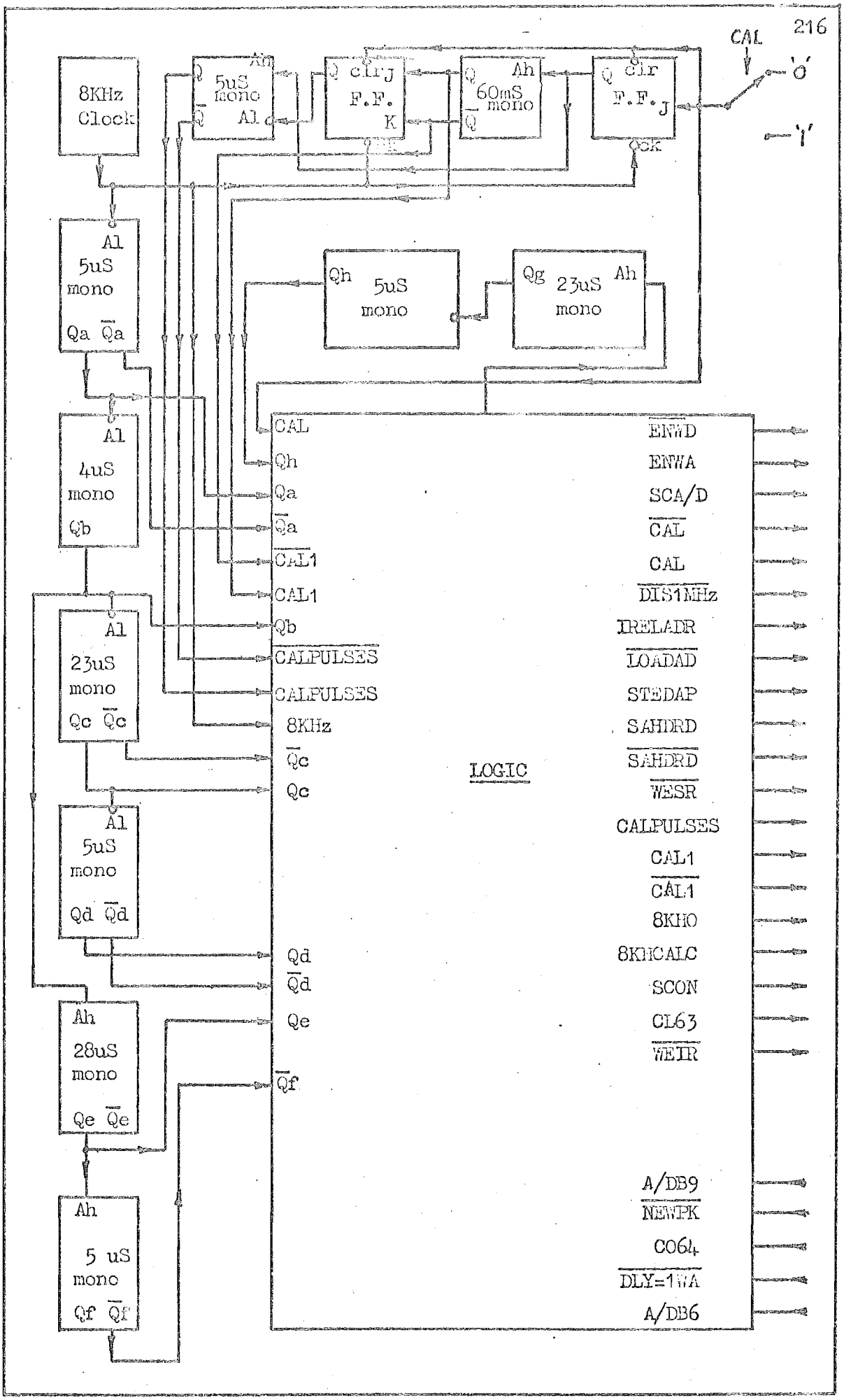


Figure A4.5 Control Board Block Diagram.

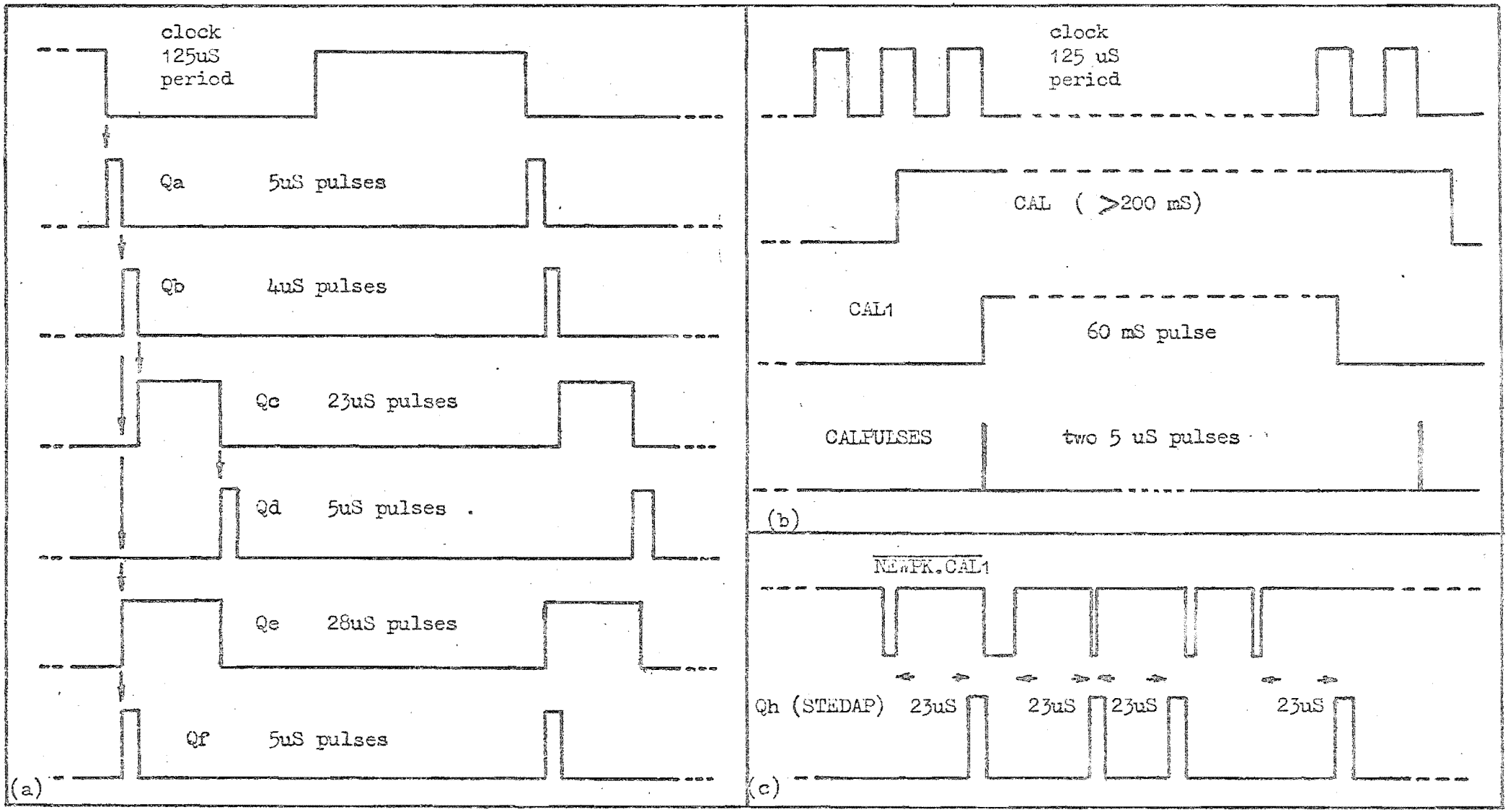


Figure A4.6 (a) 8KHz Timing Diagram. (b) Calibration Timing Diagram. (c) Impulse Response Peak Storage Timing.

Also originating from this board are the two 5 uS calibration pulses (4) and the 60 mS rectangular pulse (CAL1) indicating the first cycle of calibration. These pulses are synchronised to the 8 KHz clock by means of a dual J.K. flip-flop (3) and are illustrated in Fig. A4.6(b).

Another signal generated using monostable multi-vibrators (11) is the signal 'STEDAP' (Qh) to store the echo delay and peak value of the unscaled impulse response. This is initiated by an indication ($\overline{\text{NEWPK}}$) of a new peak occurring. A diagram of this timing cycle appears in Fig. A4.6(c).

All other signals are generated using logical combinations of these timing pulses and various status signals. A brief explanation of control signals is given here:

(1) Incoming Control Signals

A/DB9 — This is the 9 th bit out of the A/D converter and is used for short cycling the A/D converter to 8 bit operation during calibration.

$\overline{\text{NEWPK}}$ — This is an active low signal indicating that a new peak has occurred during the first half of the calibration cycle. It is used to generate a control signal for storing the peak value of the unscaled impulse response.

C064 — This indicates that the impulse response RAM address counter has reached 64. This means

either the end of the storage of impulse response samples during calibration or the end of the read cycle and is used to dissable the 1 MHz read timing.

$\overline{\text{DLY=1WA}}$ This indicates that sufficient delay has not yet been incurred before non zero samples of the impulse response appear for storage during the second phase of calibration. The write address increments and samples are stored when this goes low.

A/DB6 Bit 6 from A/D converter used for short cycling to 5 bits during normal operation.

(2) Outgoing Control Signals

$\overline{\text{ENWD}}$ Active low, connects write data to tri-state BUS for input to signal RAM.

ENWA Connects signal RAM write address from relative addressing board to parallel load inputs of address counter on the convolution board. All other times the first read address is present.

SCA/D Connects either A/DB9 or A/DB6 to the short cycle input on the A/D converter.

CAL Assynchronous calibration signal generated by switch when circuit in calibration mode.

$\overline{\text{DIS1MHz}}$ Active low, dissables 1 MHz clock when read cycle completed.

IRELADR Increments relative address counter on relative addressing board each sample period.

$\overline{\text{LOADAD}}$ Active low, loads signal RAM address counter with either write address or first read address.

STEDAP Orders storage of peak value of unscaled impulse response on interface board and the delay to that peak on the relative addressing board.

SAHDRD Output (Qa) operates sample and hold circuits.

$\overline{\text{SAHRD}}$ Clears integrator on convolution board.

$\overline{\text{WESR}}$ Active low ($\overline{\text{Qc}}$) write control (R/$\overline{\text{W}}$) for signal RAM.

CALPULSES Two 5 uS pulses spaced by 60 mS and synchronised to the 8 KHz clock for calibration purposes.

CAL1 Indicates first 60 mS of calibration cycle.

8KHO 8 KHz clock output.

8KHCALC 64 8 KHz pulses for incrementing impulse response RAM address counter during calibration.

SCON Start conversion pulse to activate A/D converter.

CL63 Clears impulse response RAM address counter prior to each read cycle.

$\overline{\text{WEIR}}$ Active low write control (R/$\overline{\text{W}}$) for impulse response RAM.

V RELATIVE ADDRESSING BOARD

This section (see Fig. A4.7) of the filter provides for the calculation of the relation between the write and first read address. This of course will depend on the delay present in the echo path. The difference between the two addresses, being the number of sample periods of the response prior to the active period.

The calculation is carried out as follows:

It is known that the active period of the impulse response is from 1 mS (8 sample periods) before the response peak, to 7 mS after it. By starting the counter (13,14) at -8 during the first cycle of calibration and storing its value at the time of the largest peak, the delay to the first sample required of the active period will be calculated. This delay is stored for the duration of the telephone call and gives the relation between the write and first read address.

When writing impulse response samples into RAM the address counter on the convolution board is not incremented (8KHCALC) until the delay measured by incrementing the counter (13,14) on this board has reached the stored delay (when $\overline{\text{DLY=1WA}}$ goes low).

During normal operation once calibration is completed the counter on this board decrements once every sample period. The output of the counter represents the write address for loading into the signal RAM address counter on the convolution board. The first read address is also available from

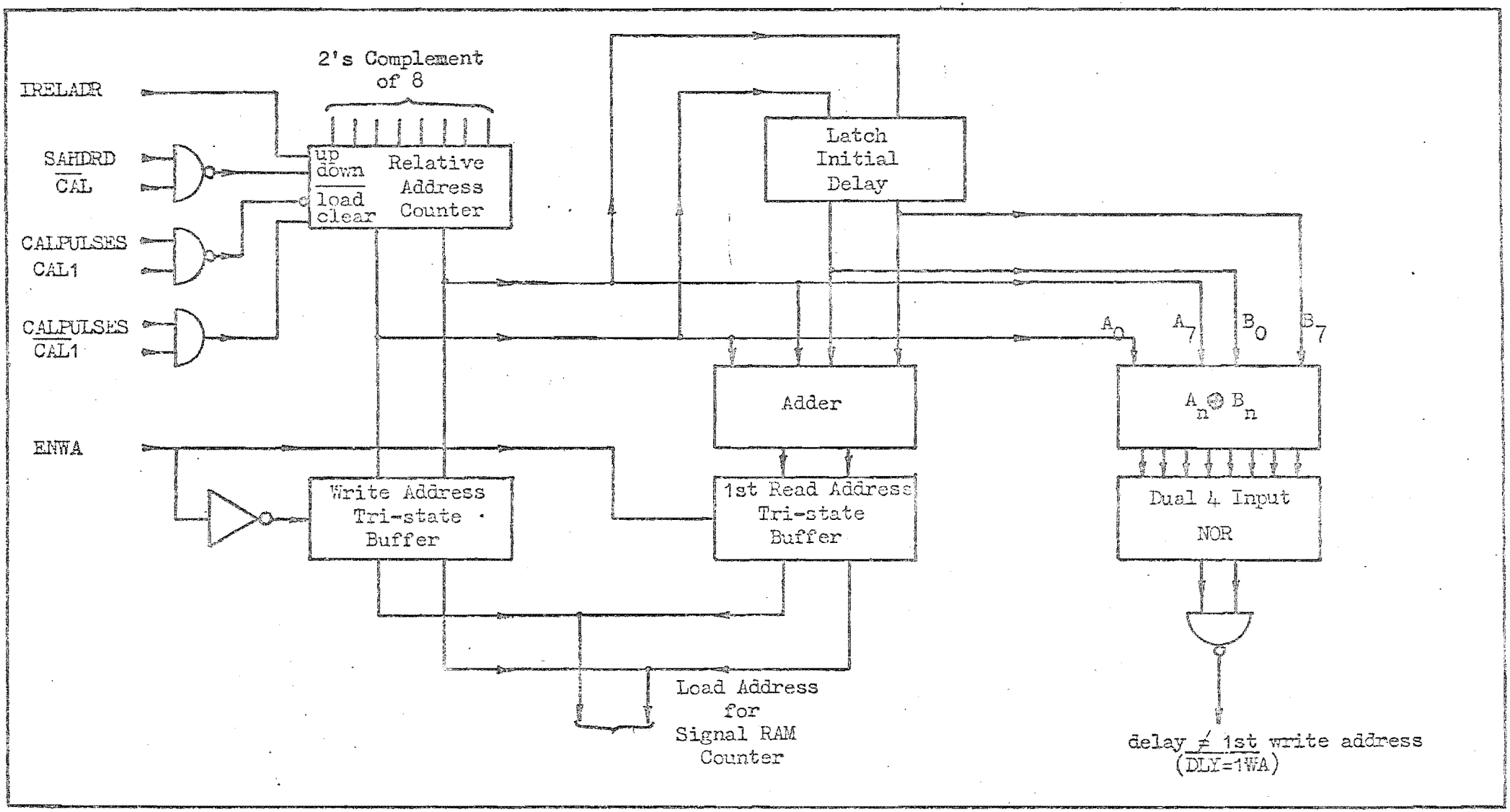


Figure A4.7 Relative Addressing Board Block Diagram.

the addition (7,8) of the write address (13,14) and the delay (15,16). The choice of either address is by way of tri-state buffers (2,3,4) onto the parallel load address connections to the convolution board.

PART 2

ECHO CANCELLER DETAILS

This appendix provides complete circuit diagrams, and where it is considered necessary detailed descriptions of circuit operation. The circuit diagrams will be given in the form of circuit board wiring following as close as possible the physical board layout. Integrated circuits are shown as numbered blocks according to their position on the board for reference purposes. Sketches of the function of the integrated circuit will appear on the diagram where possible but further details are available from manufacturers data.

Wiring lists will also be shown to give details of wiring between circuit boards.

I ANALOGUE BOARD

Reference should be made to the circuit diagram in Fig. A4.8 and the block diagram in Fig. A4.2. External connections to the board are listed in table A1.

The analogue board consists of uA 747 dual operational amplifiers, three analogue switches and a uA 795 analogue multiplier connected as a divider.

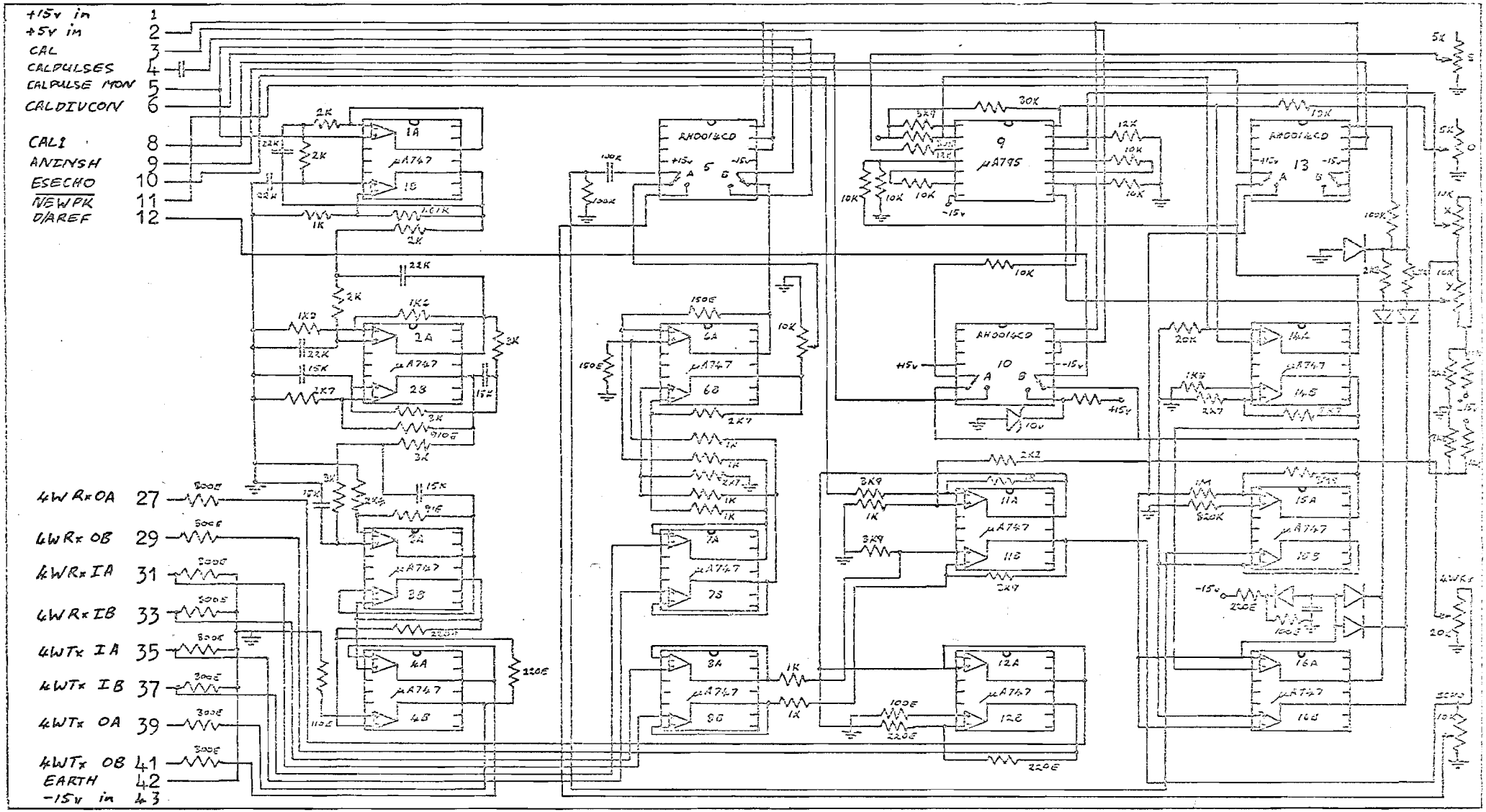


Figure A4.8 Circuit Diagram for Analogue Board

Socket No: 1 Name ANALOGUE BOARD

Pin	Signal Name	Destination							
		SKT	PIN	SKT	PIN	SKT	PIN	SKT	PIN
1	+ 15v	5		4		3		2	2
2	+ 5v (external)								
3	CAL				11				
4	CALPULSES				25				
5									
6	CALDIVCON								8
7									
8	CAL1				26				
9	ANINSH								35
10	ESECHO								21
11	NEWPK				13				
12	D/AREF								6
13									
14									
15									
16									
17									
18									
19									
20									
21									
22									
23									
24									
25									
26									
27	4W Rx OA								
28									
29	4W Rx OB								
30									
31	4W Rx IA								
32									
33	4W Rx IB								
34									
35	4W Tx IA								
36									
37	4W Tx IB								
38									
39	4W Tx OA								
40									
41	4W Tx OB								
42	EARTH								
43	- 15v								42

EXTERNAL CONNECTIONS

Table A1

The 3.5 KHz low pass filter (1B,2,3A) is buffered at the input and output by voltage followers (1A,3B).

The through transmit path enters (7A,7B), is attenuated by 16.7 dB (6A), passes through the analogue switch (5B) to the low pass filter and is converted back to 600Ω balanced (4A,4B).

The signal entering the canceller is subject to 8.6 dB gain (6B) and gain control, passes through an analogue switch (5A), buffer (15B) to the divider gain control (9,14A) or peak detector (14B,16A,16B). The signal out from the divider passes through switch (13A) to the interface board.

The output from the peak detector is subjected to 12 dB gain from an inverting amplifier (15A) and passes either to the interface board as D/AREF (10B) or to the divider as gain control (10A). Otherwise the peak detector output can pass directly to the interface board as ANINSH through switch (13A).

The receive through path enters (8A,8B), is subjected to 12 dB gain (11B) and passes to the differential amplifier (11A) for echo cancellation, is converted to a 600Ω balanced signal path (12A,12B). It should be noted that the sample and hold circuit has not yet been incorporated in the through receive path.

Apart from signal and gain controls several pre-set adjustments are provided for the divider circuit. These are; Scale Factor, Output Offset, X Offset and Y Offset and should be adjusted in accordance with manufacturers recommendations.

II INTERFACE BOARD

Reference should be made to the circuit diagram in Fig. A4.9 and the block diagram in Fig. A4.3. External connections are illustrated in table A2.

The analogue input ANINSH enters the board on pin 35 and is sampled and held by the Datel SHM-IC-1 (8) connected as an inverter with unity gain. The T.T.L. control signal SAHDRD enters on pin 34 and is a 5 uS pulse with an 8 KHz repetition rate.

The sampled and held signal at pin 7 enters the A/D converter on pin 24 with the Datel ADC-HX12BGC being connected for the +/- 2.5v bipolar range with the internal buffer disconnected. The A/D converter provides complementary offset binary code and is zeroed for an output of '10000000'. This means the least significant 7 bits represent the magnitude of the negative input voltage when the peak detector output is being converted. During the measuring of the peak detector magnitude for storage by the 9308 latch (14), the A/D converter is short cycled to 8 bits by the control board circuitry otherwise it is short cycled to 5 bits.

The 9308 latch (14) stores the peak magnitude of the unscaled impulse response according to the control signal $\overline{\text{STEDAP}}$ which enters on pin 32 and is inverted (3) on the board. The output from the latch is D/A converted by the Datel DAC-IC8BC (9) and a uA 741C amplifier (13), which provides a maximum of 2 mA reference current for the main

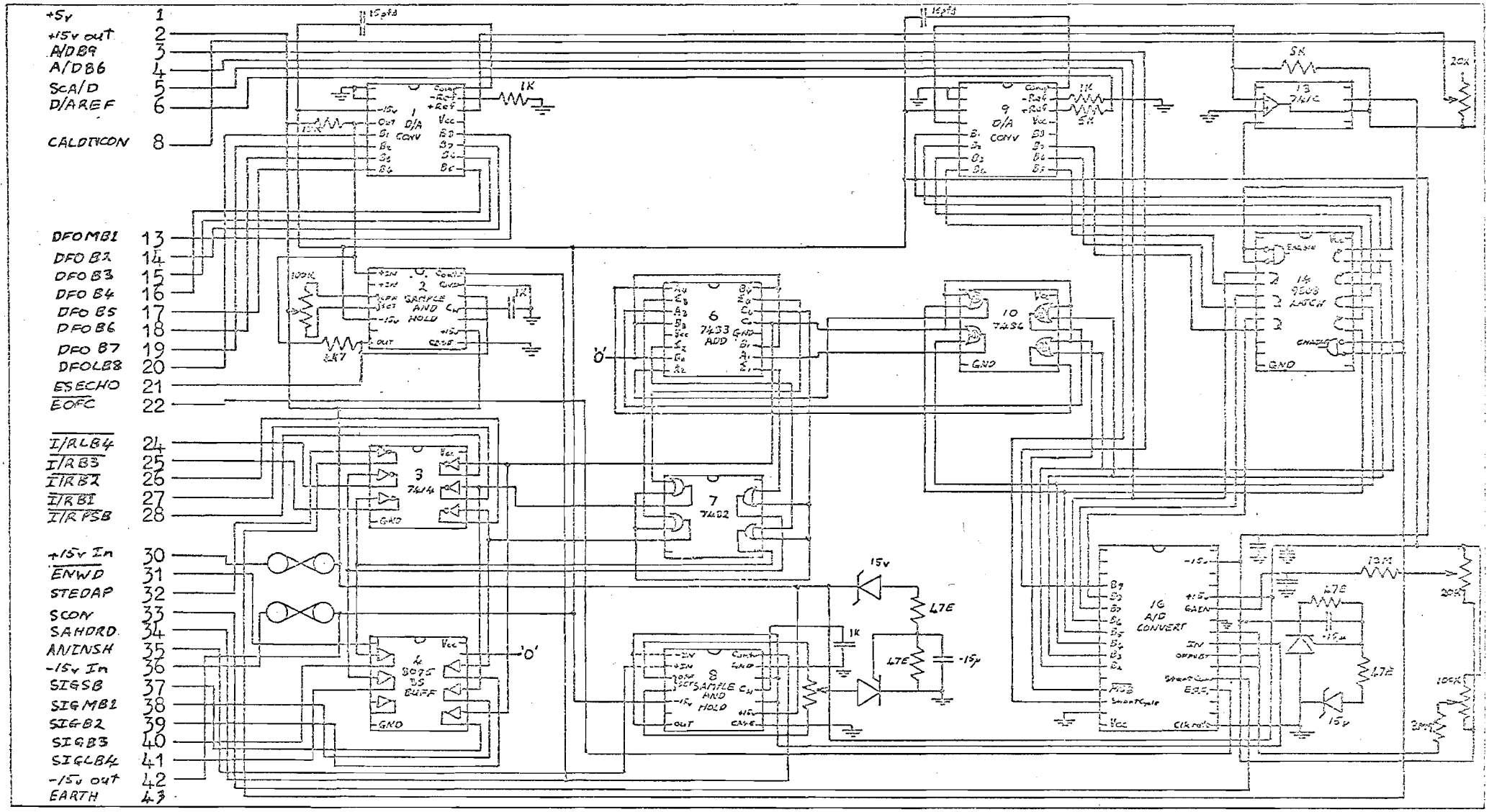


Figure A4.9. Circuit Diagram for Interface Board

Socket No: 2 Name INTERFACE BOARD 230

Pin	Signal Name	Destination							
		SKT	PIN	SKT	PIN	SKT	PIN	SKT	PIN
1	+ 5v (external)	5		4		3		1	
2	+ 15v (protected)								1
3	A/DB9				2				
4	A/DB6				34				
5	SCA/D				9				
6	D/AREF								12
7									
8	CALDIVCON								6
9									
10									
11									
12									
13	DFOMB1						8		
14	DFOB2						9		
15	DFOB3						10		
16	DFOB4						11		
17	DFOB5						12		
18	DFOB6						13		
19	DFOB7						14		
20	DFOLB8						15		
21	ESECHO								10
22	$\overline{\text{EOFC}}$								
23									
24	$\overline{\text{I/RLB4}}$						21		
25	$\overline{\text{I/RB3}}$						22		
26	$\overline{\text{I/RB2}}$						23		
27	$\overline{\text{I/RB1}}$						24		
28	$\overline{\text{I/RFSB}}$						25		
29									
30	+ 15v (external)								
31	$\overline{\text{ENED}}$				3				
32	STEDAP				18				
33	SCOH				33				
34	SAHERD				19				
35	ANINSH								9
36	- 15v (external)								
37	SIGSB						28		
38	SIGMB1						29		
39	SIGB2						30		
40	SIGB3						31		
41	SIGLB4						32		
42	- 15v (protected)								43
43	EARTH								

Table A2

D/A converter (1) for the filter output. The reference current D/AREF for the former D/A converter (9) is provided by the analogue board and is constant during calibration but proportional to the peak value of the signal during normal operation. The D/A converter (9) also provides the control voltage (CALDIVCON) for the divider gain adjustment during calibration. This is a maximum of 10v for full scale digital input.

The D/A converter (1) for the digital filter output is wired for 8 bit operation with an offset current of 1 mA provided at the output for bipolar operation, the output being connected to the sample and hold circuit (2). The sample and hold circuit is connected for current to voltage conversion with a maximum range of +/- 4.7v for +/- 1 mA input from the D/A converter and offset current. The analogue output ESECHO leaves the board on pin 21 for analogue subtraction.

During normal operation the 5 bit digital samples from the A/D converter are transformed to sign and magnitude format by the quad exclusive OR circuit (10) and the 4 bit adder (6) with the quad OR (7) being used to set the magnitude to maximum for an overflow out of the adder. This sign and magnitude representation is inverted (3) for input to the impulse response RAM as the output from the RAM is the complement of the input. Tri-state buffering is provided (4) onto the signal RAM input/output BUS with the active low control $\overline{\text{ENWD}}$ being the enabling signal during the write cycle. The sign and magnitude format has the

+ve sign bit high.

Several standard potentiometer adjustments are provided in accordance with requirements for the A/D converter and sample and hold circuits. The only other adjustment is the D/A reference current which is set for 2 mA with full scale digital input to the D/A converter (9) and 2 mA reference current into the D/A converter (9).

Power supply over voltage protection on the +/- 15v supplies is provided for the protection of the expensive D/A converter. This is achieved using S.C.R.'s across each 15v rail to earth. If the zener voltage between gate and rail is exceeded the S.C.R. will trigger and blow the supply fuse. This protected +/- 15v supply also goes to the analogue board.

III CONVOLUTION BOARD

Reference should be made to the circuit diagram in Fig. A4.10 and the block diagram in Fig. A4.4. External connections are shown in table A3. This board is relatively complex and the description will concentrate firstly on the processing of the signal and impulse response samples through to the filter output. An explanation of timing and control signals will follow.

The impulse response samples are stored in a 64 x 9 random access memory (3) - Signetics Type 82S09 which has separate input and output ports. The output of the RAM is the complement of the input and is coded in sign and magnitude format with the positive sign bit high. The signal

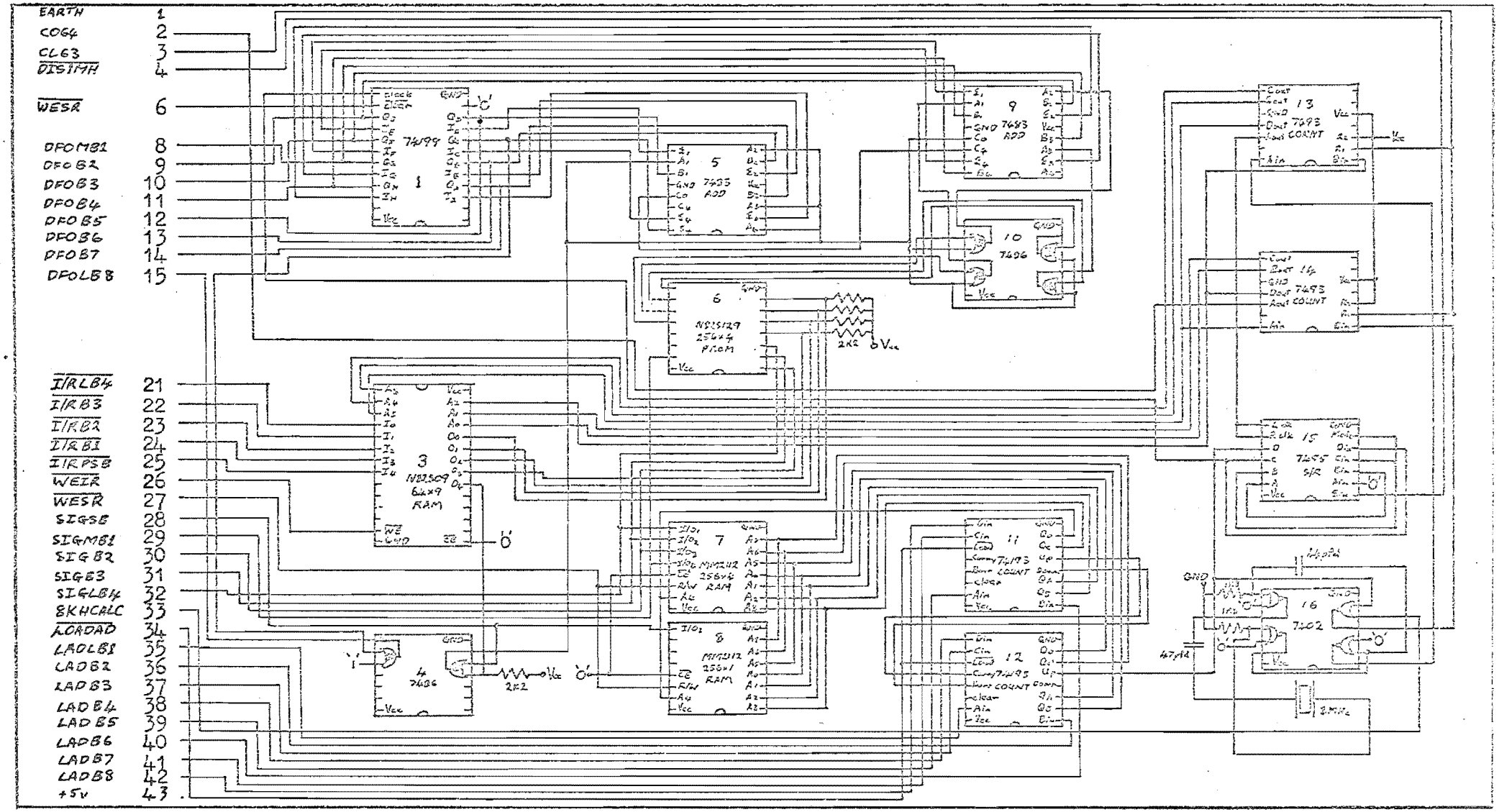


Figure A4.10. Circuit Diagram for Convolution Board

Socket No: 3 Name CONVOLUTION BOARD 234

Pin	Signal Name	Destination							
		SKT	PIN	SKT	PIN	SKT	PIN	SKT	PIN
1	EARTH	5	43	4	43	2	43	1	42
2	C064				15				
3	CI63				35				
4	$\overline{\text{DIS1MI}}$				14				
5									
6	$\overline{\text{WESR}}$				21				
7									
8	DFOMB1						13		
9	DFOB2						14		
10	DFOB3						15		
11	DFOB4						16		
12	DFOB5						17		
13	DFOB6						18		
14	DFOB7						19		
15	DFOLB8						20		
16									
17									
18									
19									
20									
21	$\overline{\text{I/RLP4}}$						24		
22	$\overline{\text{I/RB3}}$						25		
23	$\overline{\text{I/RB2}}$						26		
24	$\overline{\text{I/RB1}}$						27		
25	$\overline{\text{I/RISB}}$						28		
26	$\overline{\text{WEIR}}$				36				
27	$\overline{\text{WESR}}$				21				
28	SIGSB						37		
29	SIGMB1						38		
30	SIGB2						39		
31	SIGB3						40		
32	SIGLB4						41		
33	8KHCALC				32				
34	$\overline{\text{LOADAD}}$				17				
35	LADLB1		41						
36	LADB2		39						
37	LADB3		37						
38	LADB4		35						
39	LADB5		33						
40	LADB6		31						
41	LADB7		29						
42	LADB8		27						
43	+5V								

Table A3

samples are stored in two National M2112 256 X 4 RAM's with the samples also coded in sign and magnitude format. The signal RAM's (7,8) have common input/output ports and read data is only valid when the R/$\overline{W}$ control is high according to specifications.

The 4 bits representing sample magnitudes from each RAM are used to address the permanently enabled Signetics Type N82S-129 PROM (6). This 256 X 4 PROM whose address is formed by two 4 bit words representing the magnitudes of the pair of samples is programmed to have an output proportional to the magnitude of the product of the pair of samples. The constant of proportionality is 1/15 so as to utilise the full 16 output levels available. As already mentioned the PROM is permanently enabled and only the address changes with the data being valid 35 nS after the address has stabilised.

The sign bits are checked for dissimilarity out of the RAM's using an exclusive OR gate (13A) whose output complements the product of two dissimilarly signed magnitudes using a quad exclusive OR gate (7). If complementing is required the carry bit into the 4 bit adder (8) is taken high as are the 4 input bits to the other 4 bit adder (12). This results in the 2's complement of the product being added to the interim total which amounts to subtraction as the product was negative.

The only synchronous part of the read cycle occurs at the accumulator which is in the form of a 74199 parallel

load shift register (16). The output from the adders is clocked into the shift register whose output then forms the next input to the adders ready for the next product to be added. The integrator is clocked 750 nS after the address of the RAM's has been incremented thus allowing for the address (40 nS), RAM output (500 nS), PROM output (35 nS) and adder outputs (20 nS) to settle to a stable state.

The 1 MHz timing is generated by an 8 MHz clock (16), a divide by 2 circuit (13) and a shift register (15) which provides sequential timing and an effective division by 4 to give 1 MHz. The 1 MHz timing outputs from the shift register increment the address counters (13,14 and 11,12) and 750 nS later clock the integrator.

External controls are: LOADAD which parallel loads the signal RAM address counter (11,12) : $\overline{\text{DISIMH}}$ which dissables the 1 MHz timing at the shift register following completion of the read cycle or during calibration: 8KHCALC is 64 8 KHz clock pulses for incrementing the Impulse response address counter during calibration which is otherwise 'low'. $\overline{\text{WESR}}$ and $\overline{\text{WEIR}}$ are active low write controls for the RAM's with the latter high at all times except for calibration. $\overline{\text{WESR}}$ also clears the integrator.

IV CONTROL BOARD

Operation of this board is quite straightfoward apart from the synchronisation of the calibration pulses to the 8 KHz clock. This will be explained in detail. Other signals are combinations of timing pulses Qa through Qh

and status signals. The logic is best described by listing the logical description for each output and listing the integrated circuits from which each logical expression is derived. The circuit diagram is shown in Fig. A4.11 and the block diagram in Fig. A4.5 with external connections being listed in Table A4.

The calibration signals are derived as follows:

CAL1 is a pulse of 60 mS length which goes high after the next positive and negative transition of the 8 KHz clock. This is illustrated in Fig. A4.6(b). CAL is clocked into the J-K flip-flop (3A) which activates the 60 mS monostable (4A) (CAL1) and the 5 uS monostable (4B) (CALPULSES). After the 60 mS monostable returns to rest the second J-K flip-flop is activated after the next positive and negative transition of the clock. This causes a second 5 uS pulse to be generated. This means both monostables are activated on the negative going transition of the clock pulse only, providing synchronisation.

The remaining signals are generated as follows. Reference should be made to the timing diagrams in Fig. A4.6(a) and Fig. A4.6(c).

$\overline{ENWD} = \overline{Qe \cdot \overline{Qf}}$ 13A (10A, 10B)

$ENWA = Qe$ 10A

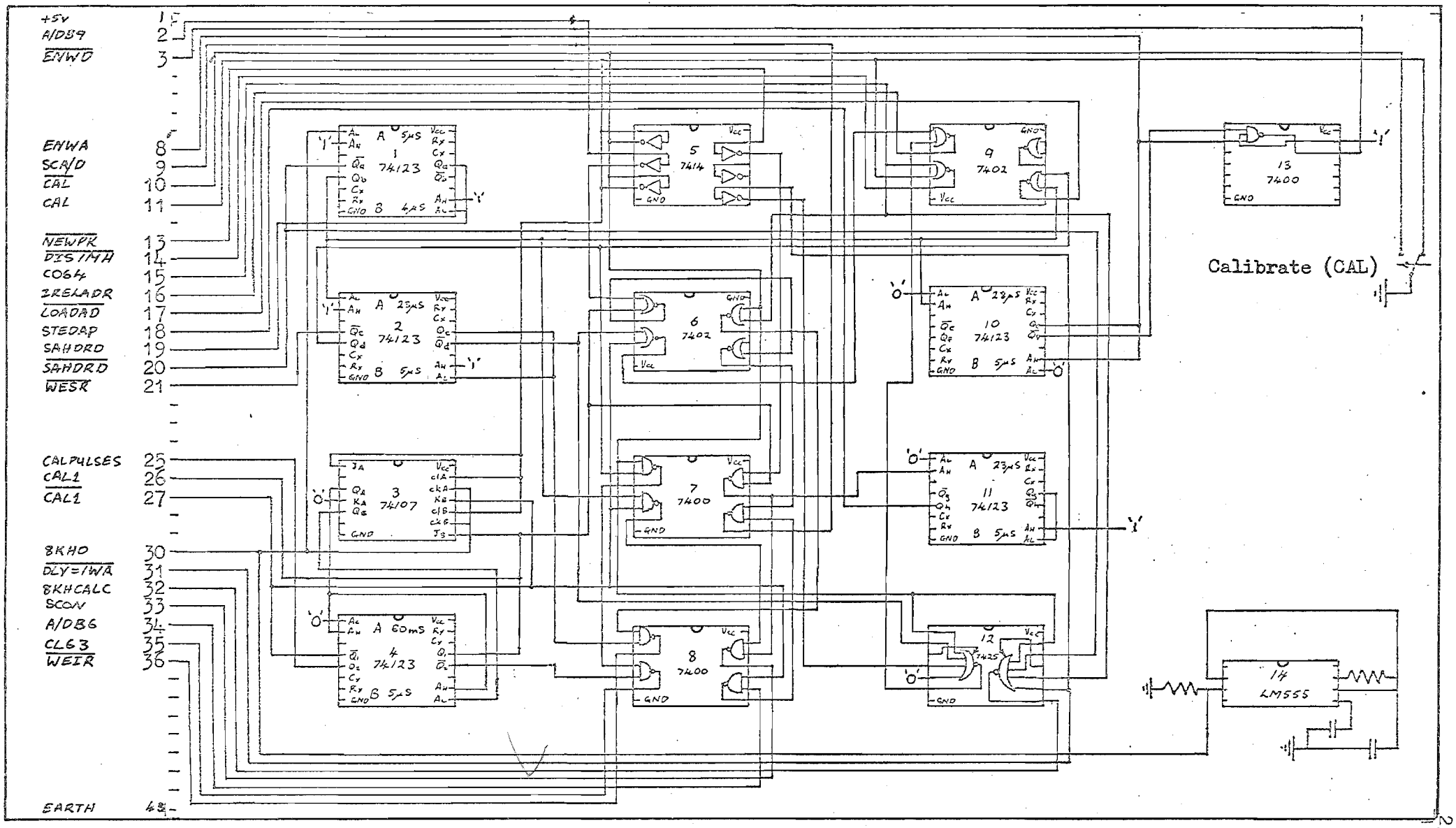


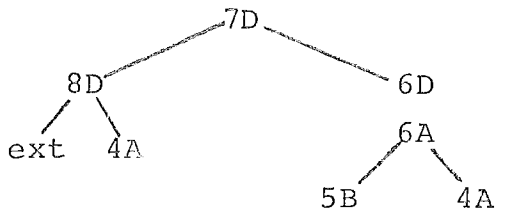
Figure A4.11. Circuit Diagram for Control Board

Socket No: 4 Name CONTROL

Pin	Signal Name	Destination							
		SKT	PIN	SKT	PIN	SKT	PIN	SKT	PIN
1	+ 5v (external)	5		3		2		1	
2	A/DB9						3		
3	$\overline{\text{ENCD}}$						31		
4									
5									
6									
7									
8	ENWA		9						
9	SCA/D						5		
10	$\overline{\text{CAL}}$		10						
11	CAL								3
12									
13	$\overline{\text{NEWPK}}$								11
14	$\overline{\text{DIS1MH}}$				4				
15	CC64				2				
16	$\overline{\text{IRELADR}}$		2						
17	$\overline{\text{LOADAD}}$				34				
18	$\overline{\text{STEDAP}}$		4				32		
19	$\overline{\text{SAHDRD}}$		8				34		
20	$\overline{\text{SAHDRD}}$		9		6				
21	$\overline{\text{WESR}}$				27				
22									
23									
24									
25	CALPULSES		3						4
26	CAL1								8
27	$\overline{\text{CAL1}}$		5						
28									
29									
30	8KHO								
31	$\overline{\text{DLY=1WA}}$		11						
32	8KHCALC				33				
33	SCON						33		
34	A/DB6						4		
35	CL63				3				
36	$\overline{\text{WEIR}}$				26				
37									
38									
39									
40									
41									
42									
43	EARTH (external)								

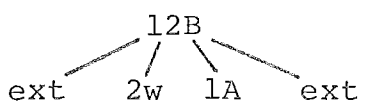
Table A4.

SCA/D = $\overline{\overline{A/DB6 \cdot \overline{CAL1}} \cdot \overline{\overline{A/DB9} + CAL1}}$



8KHCALC = $DLY=1WA \cdot CAL \cdot Qa \cdot \overline{C064}$

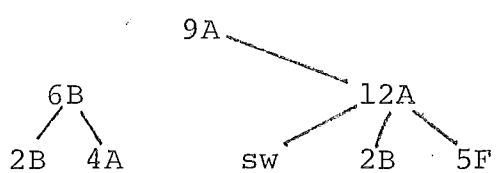
= $\overline{\overline{DLY=1WA} + \overline{CAL} + \overline{Qa} + C064}$



DIS1MH = $\overline{C064 + CAL}$ 9B

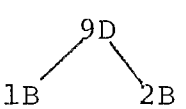
IRELADR = $\overline{Qd \cdot CAL1 + CAL \cdot Qd \cdot \overline{DLY=1WA}}$

$\overline{\overline{Qd} + \overline{CAL1} + \overline{CAL} + \overline{Qd} + DLY=1WA}$



STEDAP = $\overline{Qh}$ 11B

$\overline{LOADAD}$ = $\overline{Qb + Qd}$



SAHDRD = Qa 1A

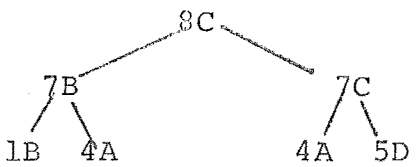
$\overline{\text{SAHDRD}}$ = $\overline{\text{Qa}}$ 1A

$\overline{\text{WESR}}$ = $\overline{\text{Qc}}$ 2A

8KH0 8 KHz clock output 16

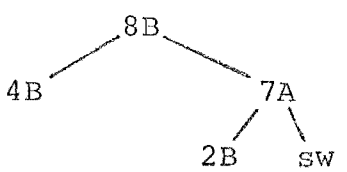
SCON = Qb . $\overline{\text{CAL1}}$ + CAL1 . NEWPK

$$= \overline{\overline{\text{Qb . CAL1}} \; . \; \overline{\text{CAL1 . NEWPK}}}$$



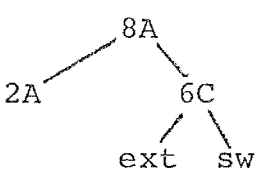
CL63 = CALPULSES + Qd . $\overline{\text{CAL}}$

$$= \overline{\overline{\text{CALPULSES}} \; . \; \overline{\text{Qd . CAL}}}$$



$\overline{\text{WEIR}}$ = $\overline{\text{Qc . C064 . CAL}}$

$$= \overline{\text{Qc . C064} + \overline{\text{CAL}}}$$



CAL Assynchronous indication of calibration from the mechanically operated switch.

V RELATIVE ADDRESSING BOARD

The circuit diagram for this board is shown in Fig. A4.12 with the block diagram in Fig. A4.7. The board employs counters, latches, adders, tri-state buffers and some general logic.

The relative addressing counter (13,14) decrements once every sample period according to the logical expression;

$$\overline{\text{decrement count}} = \overline{\text{SAHDRD . CAL}} \qquad 2B$$

This counter gives the current write address which is connected via the tri-state buffer (2,3) to the 'load address BUS' according to $\overline{\text{ENWA}}$ (5A). Otherwise the first read address which is the summation (7,8) of the write address plus delay (15,16) is connected (3,4) to this BUS according to ENWA.

The counter is loaded with '-8' prior to the measurement of the unscaled impulse response by the control;

$$\overline{\text{LOAD}} = \overline{\text{CALPULSES . CAL1}} \qquad (1A)$$

The counter is cleared by the second calibration pulse by;

$$\text{CLEAR} = \text{CALPULSES . } \overline{\text{CAL1}} \qquad (1C,1D)$$

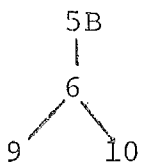
The counter is incremented by the incoming control IRELADR during calibration only.

A status output signal is provided for calibration purposes to indicate that the incurred delay during the

second phase has not reached the total delay prior to the active period. This signal is;

$$\overline{DLY=1WA} = (A_1+B_1)+(A_2+B_2)+(A_3+B_3)+(A_4+B_4)+(A_5+B_5)+(A_6+B_6)+(A_7+B_7)+(A_8+B_8)$$

$$= \overline{(A_1+B_1)+(A_2+B_2)+(A_5+B_5)+(A_6+B_6)} \cdot \overline{(A_3+B_3)+(A_4+B_4)+(A_7+B_7)+(A_8+B_8)}$$



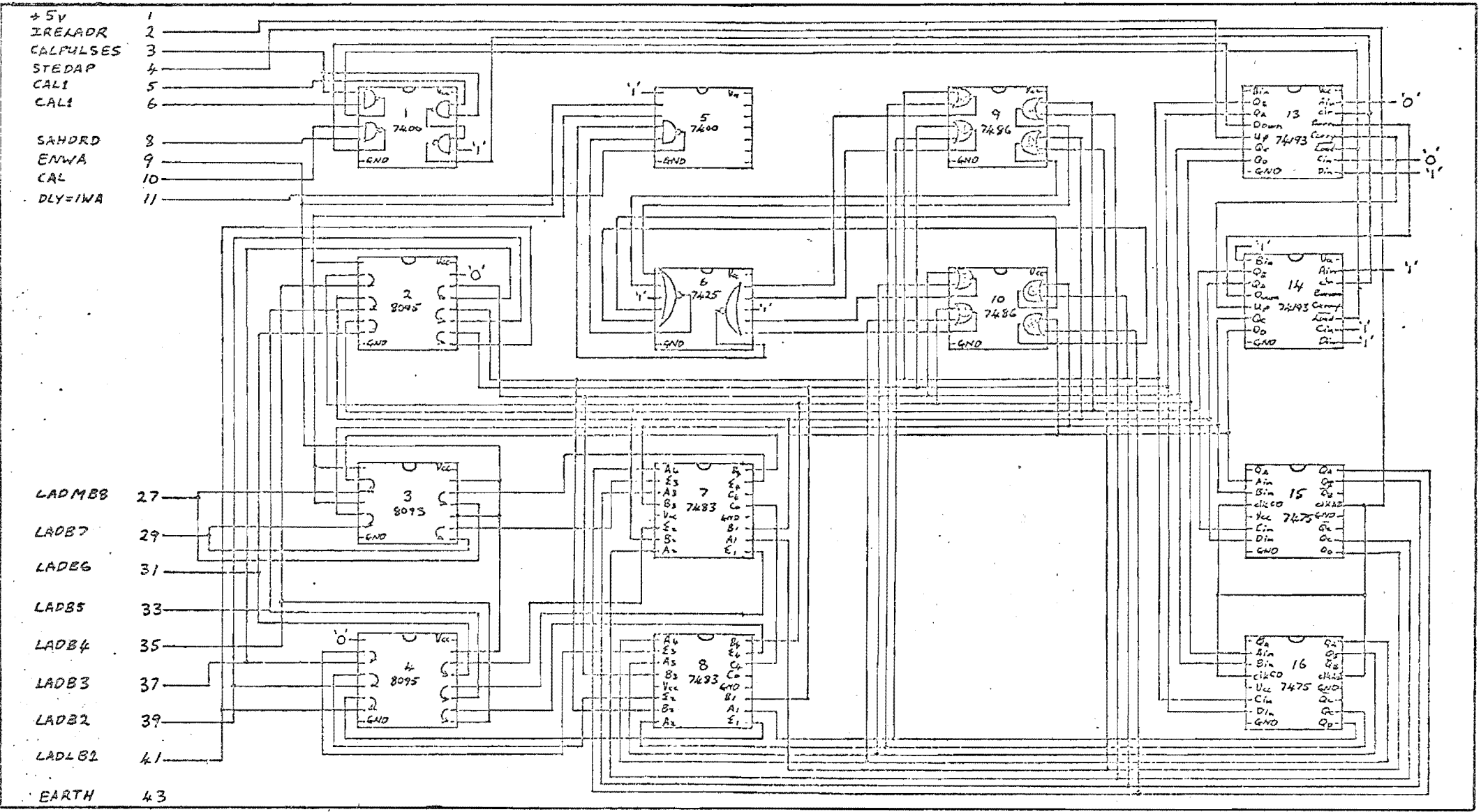


Figure A4.12 Circuit Diagram for Relative Addressing Board

Socket No: 5 Name RELATIVE ADDRESSING BOARD

Pin	Signal Name	Destination							
		SKT	PIN	SKT	PIN	SKT	PIN	SKT	PIN
1	+ 5v	4		3		2		1	
2	IRELADR		16						
3	CALPULSES		25						
4	STEDAP		18						
5	$\overline{\text{CAL1}}$		27						
6	CAL1		26						
7									
8	SAHDRD		19						
9	ENWA		8						
10	$\overline{\text{CAL}}$		10						
11	$\overline{\text{DLY=1WA}}$		31						
12									
13									
14									
15									
16									
17									
18									
19									
20									
21									
22									
23									
24									
25									
26									
27	LADMB8				42				
28									
29	LADB7				41				
30									
31	LADB6				40				
32									
33	LADB5				39				
34									
35	LADB4				38				
36									
37	LADB3				37				
38									
39	LADB2				36				
40									
41	LADLB1				35				
42									
43	EARTH (external)								

Table A5

APPENDIX V

LOGARITHMIC ECHO CANCELLER

DETAILS

Details are given for the circuitry and operation of those boards connected up for single channel operation. Boards originally designed for multiplex operation. The sections of the canceller to be discussed are;

(a) Calibration Circuitry comprising the correlator and memory boards.

(b) Analogue to Digital and Digital to Analogue conversion boards.

(c) The two channel dedicated boards for analogue and digital circuitry.

(d) The extra logic board designed subsequently to provide timing and control logic for single channel operation.

(e) Logarithmic conversion board.

(a) Calibration Circuitry

This circuitry transmits a pseudo random noise sequence of length 1023, stores the 1280 response samples in 12 bit linear format and then correlates the response with an

extended version of the transmitted sequence. Fig. A5.1. gives a diagramatic explanation of the correlation required.

An explanation of circuit operation is given with reference to Fig. A5.2 . Individual components are numbered on Fig. A5.3. and these numbers are found also on the block diagram in Fig. A5.2.

The start calibration pulse 'SCAL' generated by the logic board and synchronised to 8 KHz triggers a D Flip-Flop (12A) which clears and presets the PRN1 generator (9,10) through monostables (8A,8B). This sets the PRN1 generator to the correct start state. The PRN1 generator then increments at an 8 KHz rate with the clock originating from the logic board, until the output reaches the end of the sequence - detected b the 10 input AND gate. The D Flip-Flop (12A) is then cleared and no further transmission occurs as the analogue switches (7) are biased off. When 1280 samples of the response have been stored - determined from the address counter (3,4) on the memory board (C01280) and gates on the logic board the 'MEASURE' signal from the logic board goes low. An 'ENDMEASURE' pulse clears PRN1 (9,10) and resets it to the start state for the correlation cycle. During the measure cycle the write enable signal $\overline{\text{WERR}}$ is generated by a combination of the 'MEASURE' and channel write enable timing pulse $\overline{\text{EWT}}$.

During the correlation cycle PRN1 is then incremented every time the memory address counter reaches the end of the read cycle (C01280). For each new coefficient PRN2 (5,6) is cleared and reset through (4A,4B) to the new start state

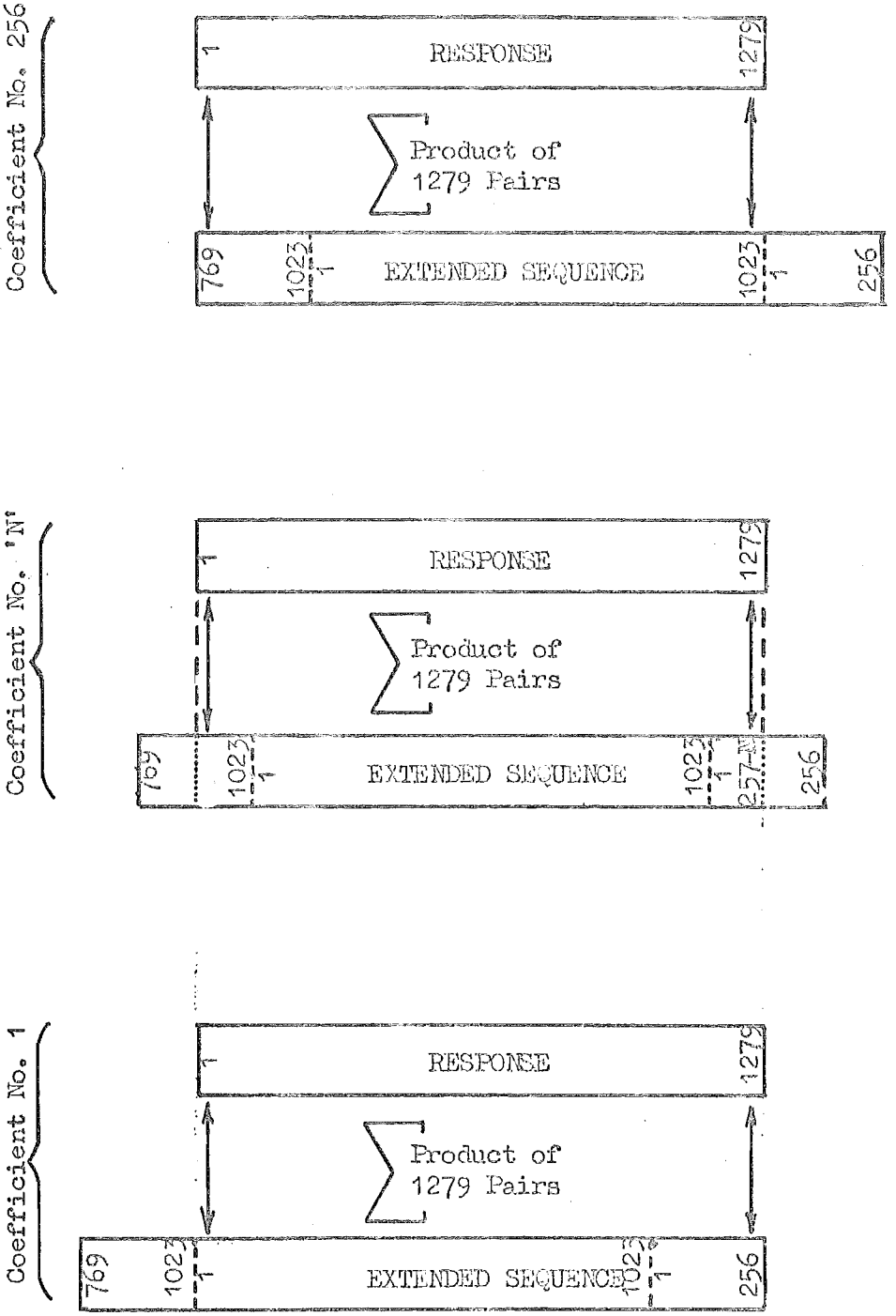


Fig. A5.1. Sequence of Coefficient Calculation by Correlation.

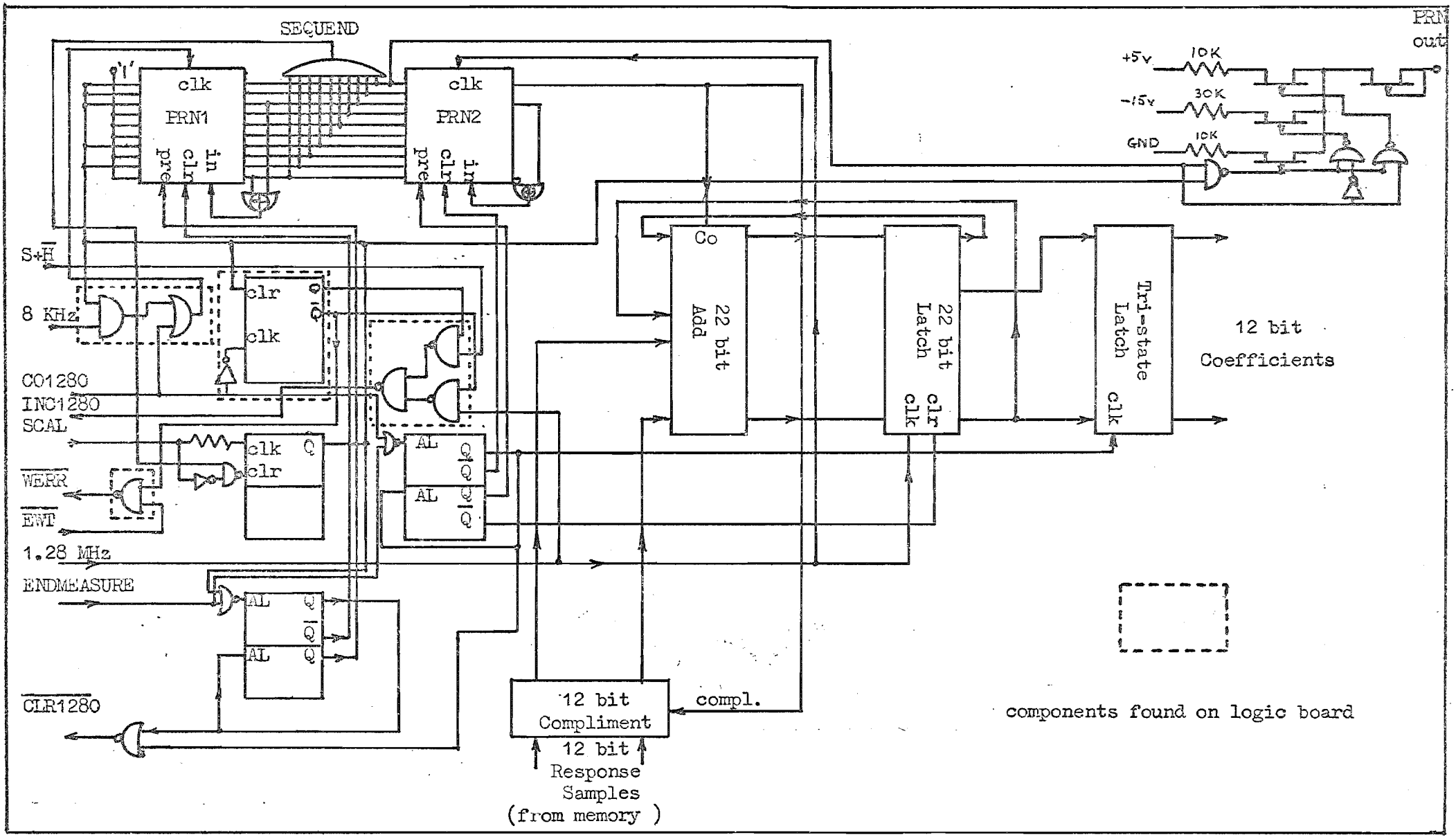


Fig. A5.2. Block Diagram of Correlator Operation.

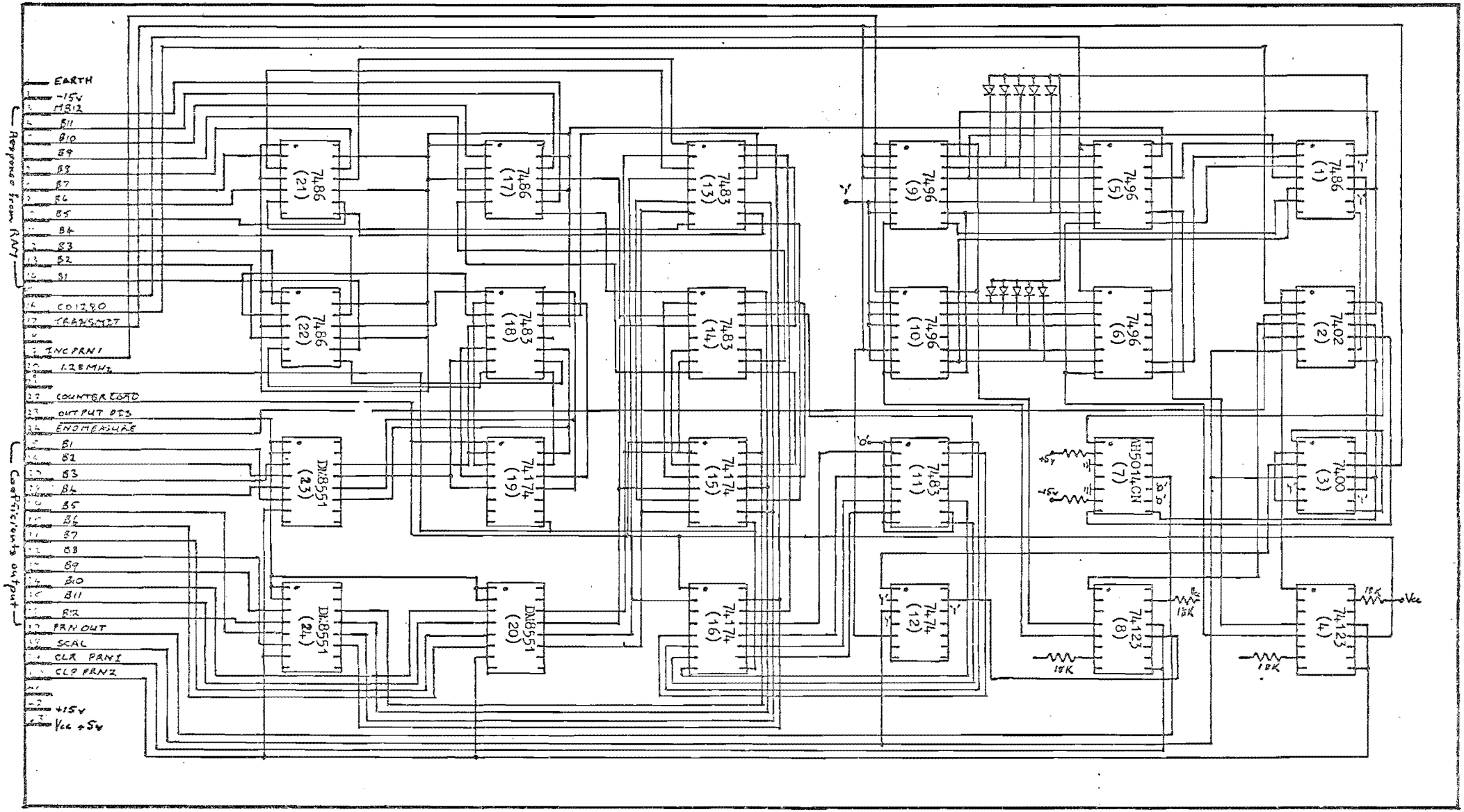


Fig. 5.3. Correlator Circuitry

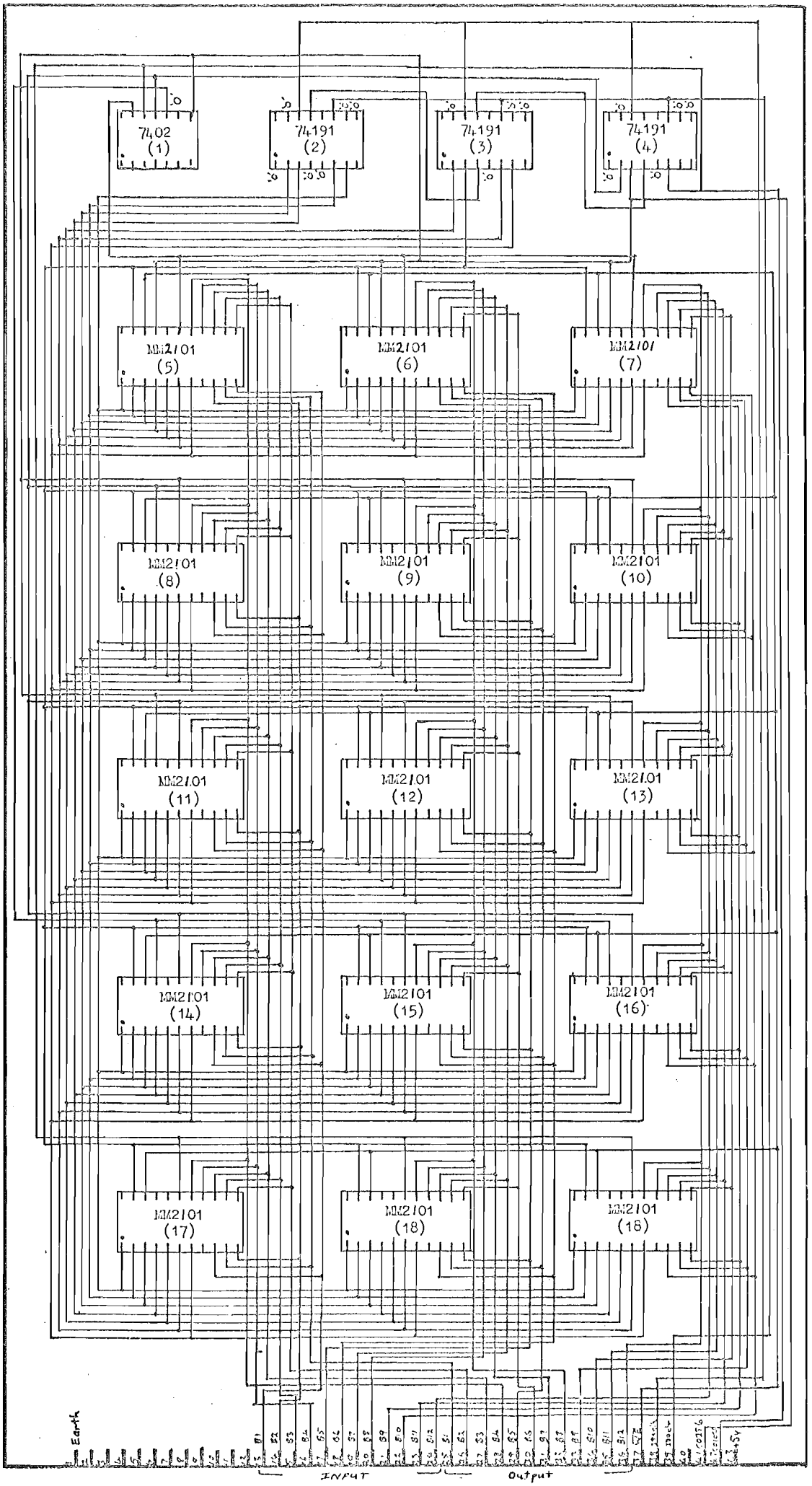


Fig. A5.4. Correlator Memory Board

provided by PRN1 (9,10). The 255 coefficients are calculated in reverse as PRN1 is stepped in one direction only. As 1280 shifts of PRN2 are required and a 1.28 MHz clock rate is used a coefficient is calculated every 1 mS. At the end of every 0 - 1279 addressing sequence the address counter is cleared by a monostable (4A).

As the address counter on the memory board increments the response samples appear at the input to the correlator. If the output of PRN2 is +ve the sample is two's complemented (17,21,22,18) before being added to the interim sum in the digital accumulator (adders and latches 11,13,14,18,15,16,19). At the end of each correlation the coefficient is available at the output of the tri-state buffers (20,23,24).

The memory board itself consists solely of 1280 bytes of 12 bits (5-19) which are selected by the address counter (2,3,4) and logic (1). All control pulses are generated external to this board.

(b) A/D and D/A Circuitry

Although these boards were initially designed to be multiplexed they are at present used as straight conversion boards for single channel operation.

A/D Conversion

The A/D board (see Figs.A5.5 and A5.6) has positions for multiplex switches (11-15), timing for multi-channel operation (3,4) and synchronising circuitry (7,8,10) and miscellaneous logic (7,8).

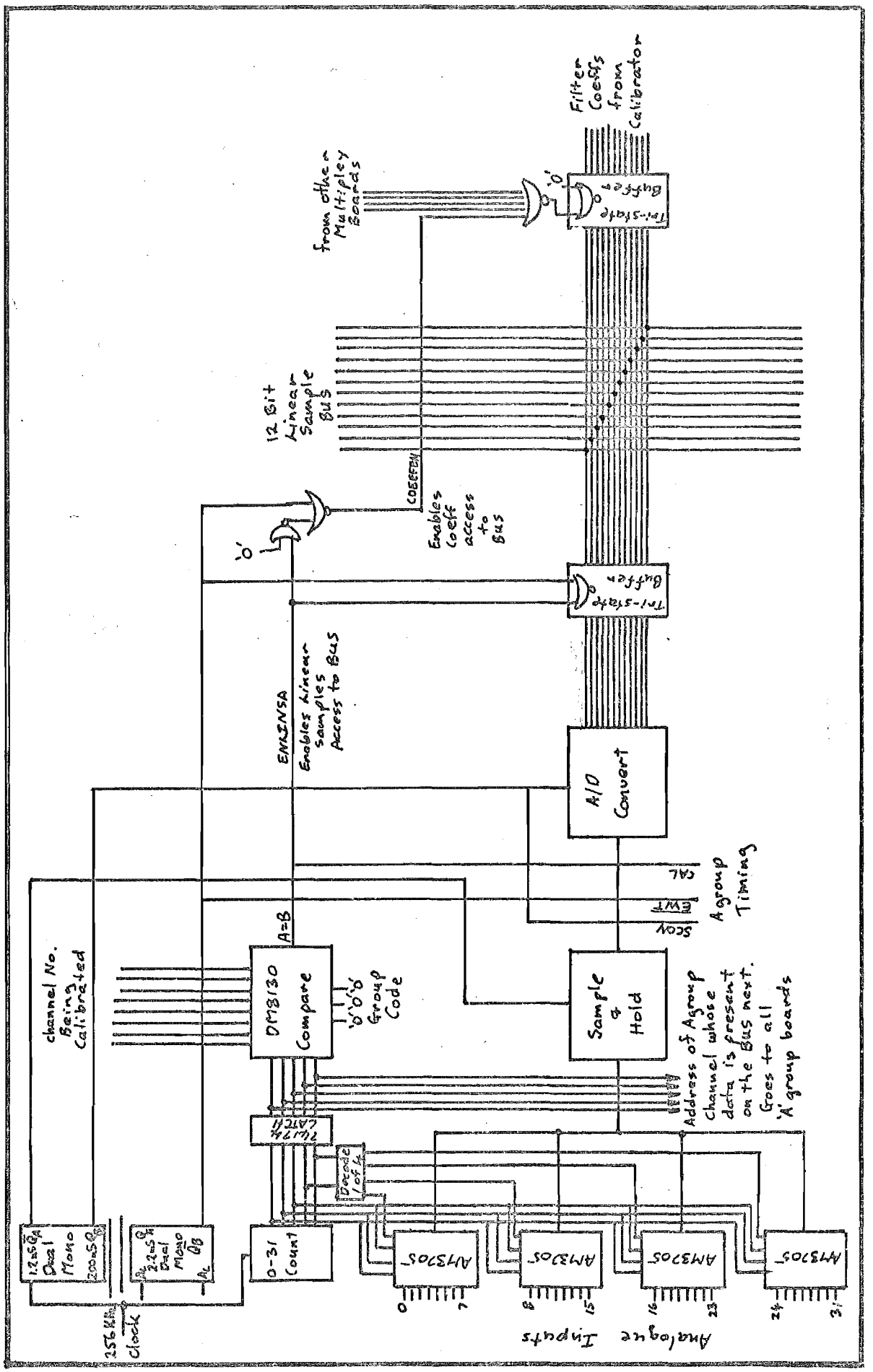


Fig. A5.5. Block Diagram of A/D Multiplexed Circuitry.

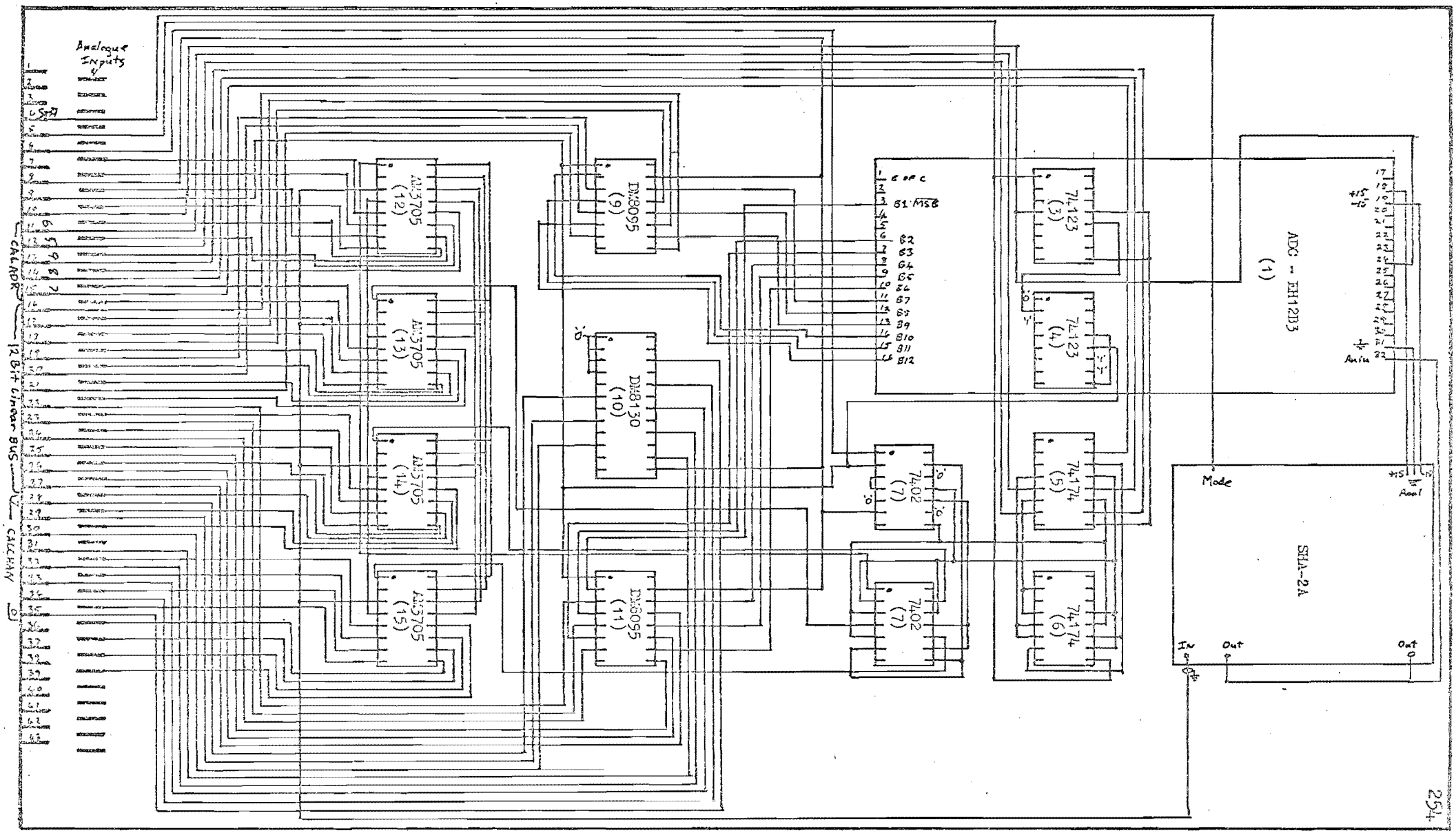


Fig. A5.6. Multiplexed A/D Conversion.

Originally the counter operating at 256 KHz incremented and selected the analogue signal to be converted. If under calibration (determined by (10)) and coefficients were being placed on the 12 bit linear 'BUS' for log conversion, signal samples were prevented from appearing by 'ENLINSA'.

For single channel operation the input from the channel analogue board goes directly to the sample and hold circuit (2) and then to the A/D convertor (1). The 12 bit output from the A/D convertor is placed on the 12 bit linear 'BUS' either for storage by the correlator or conversion by the log conversion board. When the channel is under calibration after the end of the MEASURE cycle, the 12 bit samples are prevented from appearing on the 'BUS' to allow the coefficients from the correlator to appear. At present all timing and control is generated by the supplementary logic board.

D/A Conversion

Figs. A5.7. and A5.8. relate to this circuitry. Originally this board was designed to provide de-multiplexing of the analogue output through switches (7-10), selected (5,6) by the channel address from the A/D board. At present it only provides for straight D/A conversion (1,3) for interfacing between the digital convolution board and the analogue circuit board.

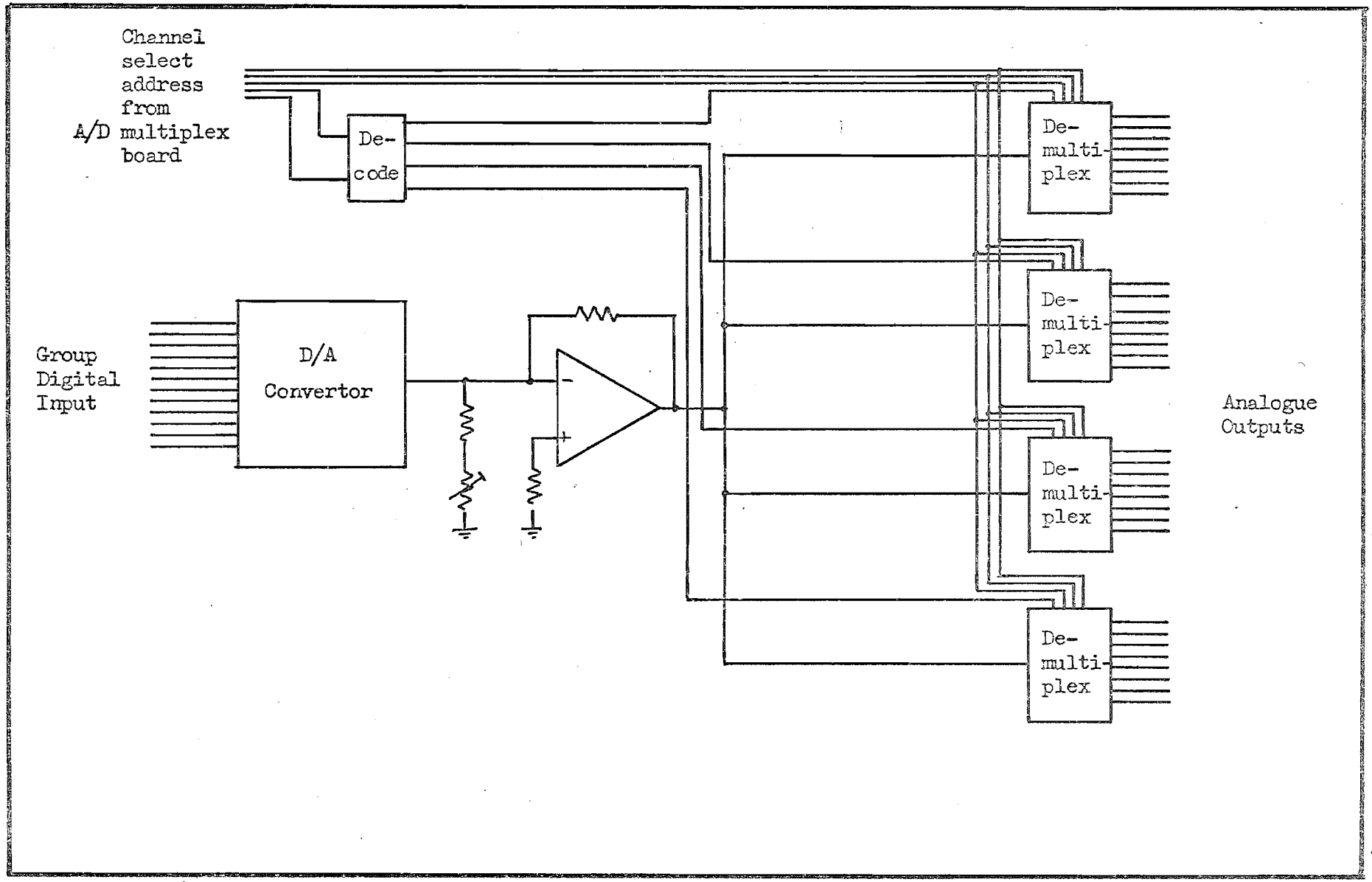


Fig. A5.7. Block Diagram of D/A Multiplexed Circuitry

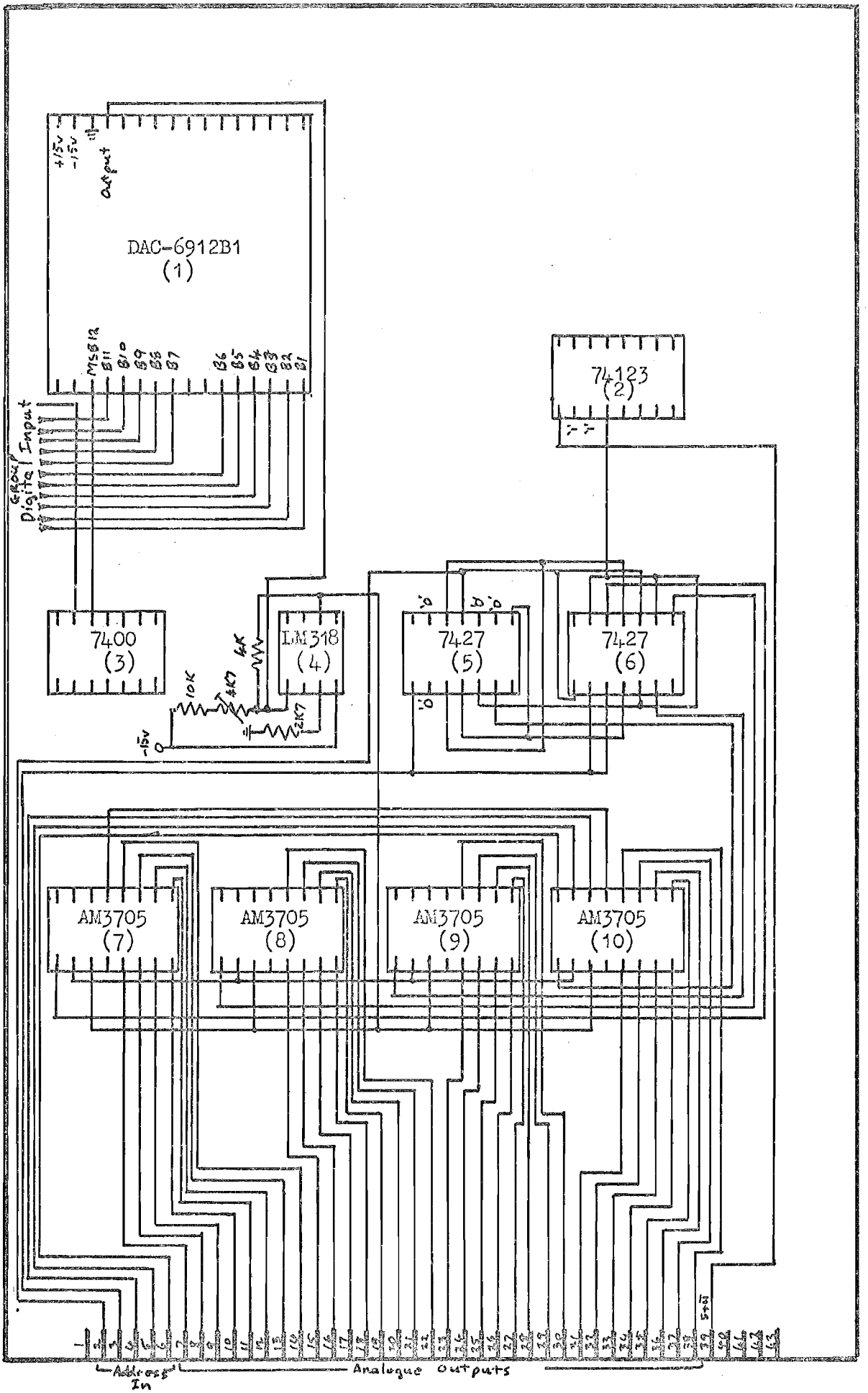


Fig. 5.8. D/A Multiplexed Circuitry

(c) Channel Dedicated Circuitry

Analogue Board

Reference should be made to Figs. A5.9. and A5.10. The incoming speech from the distant subscriber at the 4 wire receive input is amplified (1) by 15 dB to get +/- 2.5 V maximum for output to the A/D convertor board during normal operation. The summing amplifier (3) provides for the insertion of the noise sequence and an attentuation of 19 dB prior to low pass filtering (8) to elliminate the high frequencies from the sequence. The last amplifiers in this path (7,2) provide the 600 ohm balanced output at - 8 dBm for the 4 wire receive out to the near subscriber.

The transmit path performs similar functions. The incoming signal is amplified by 3 dB to provide output at +/- 2.5 V maximum to the A/D convertor board during calibration cycle. The amplifier (4) provides summing facilities for the echo estimate from the D/A board. This is then low pass filtered (9) and restored to the correct level (+4 dBm) and impedance (600) for transmission to the distant subscriber.

Convolution Board

Refer to Figs. A5.11. and A5.12. This board provides for all the processing of the digital signal and impulse response samples.

Filter coefficients are entered into memory (7,10) off the 8 bit log 'BUS' during the correlation portion of the

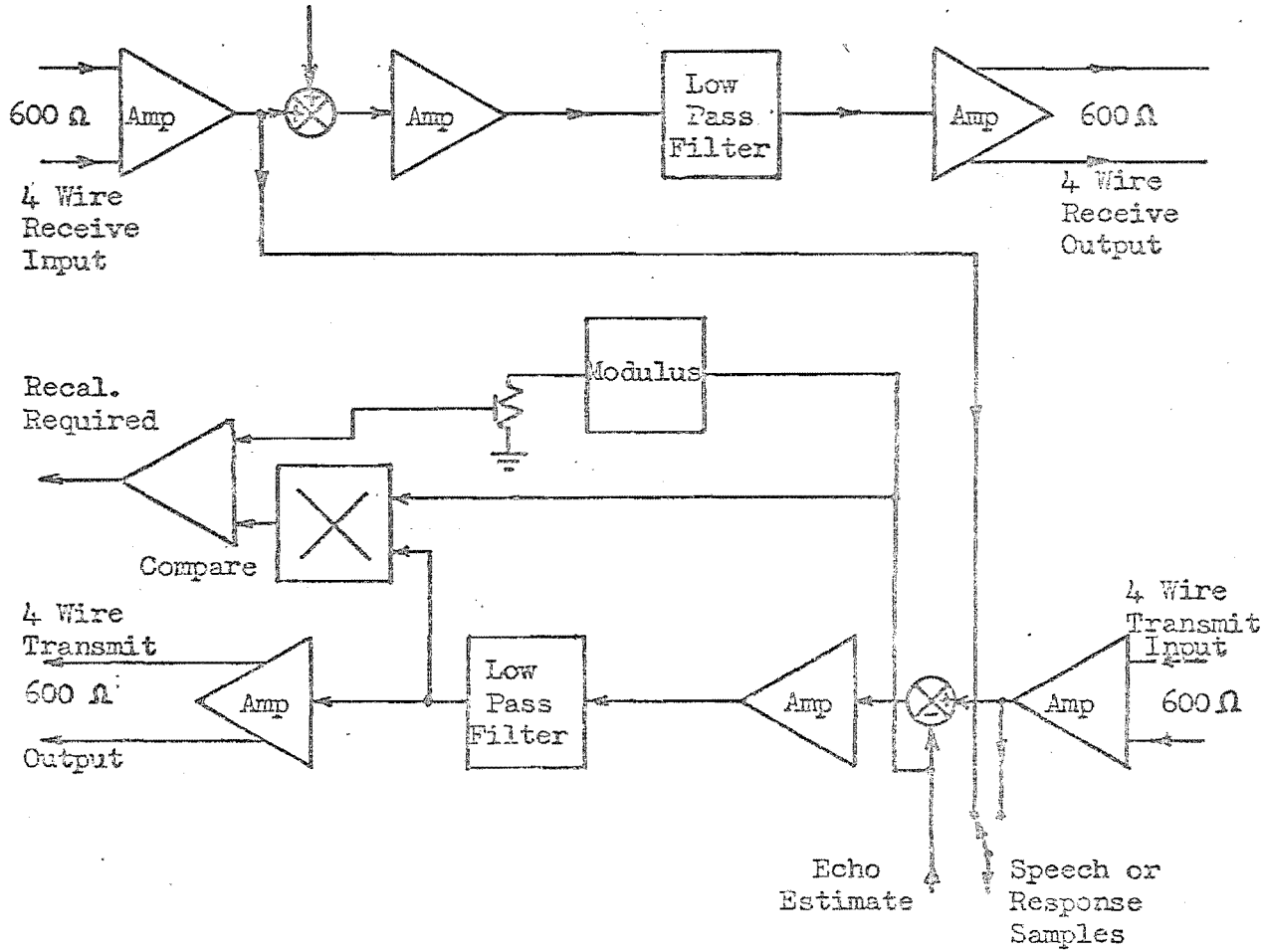


Fig. A5.9. Analogue Circuitry block diagram

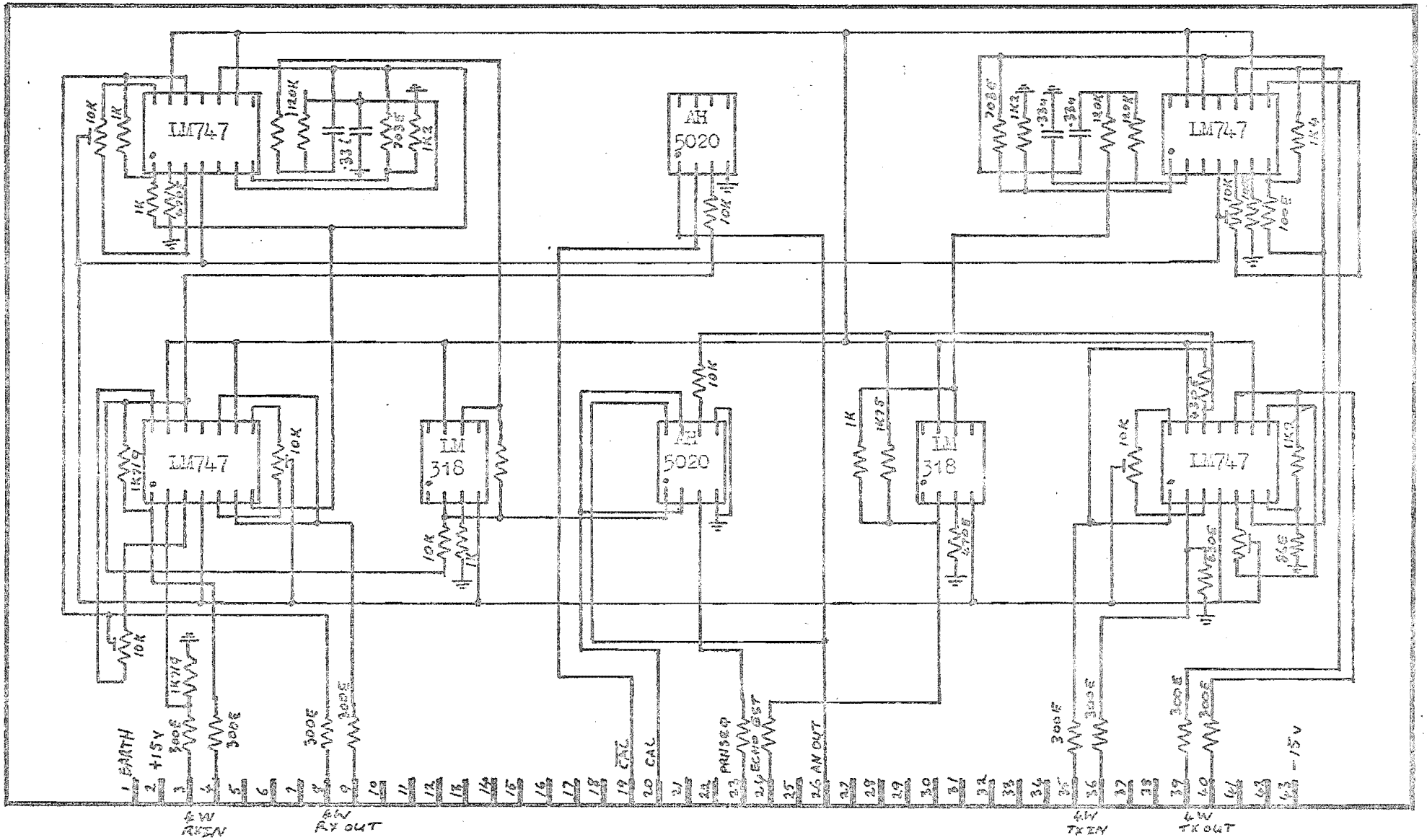


Fig. 5.10. Analogue Circuitry

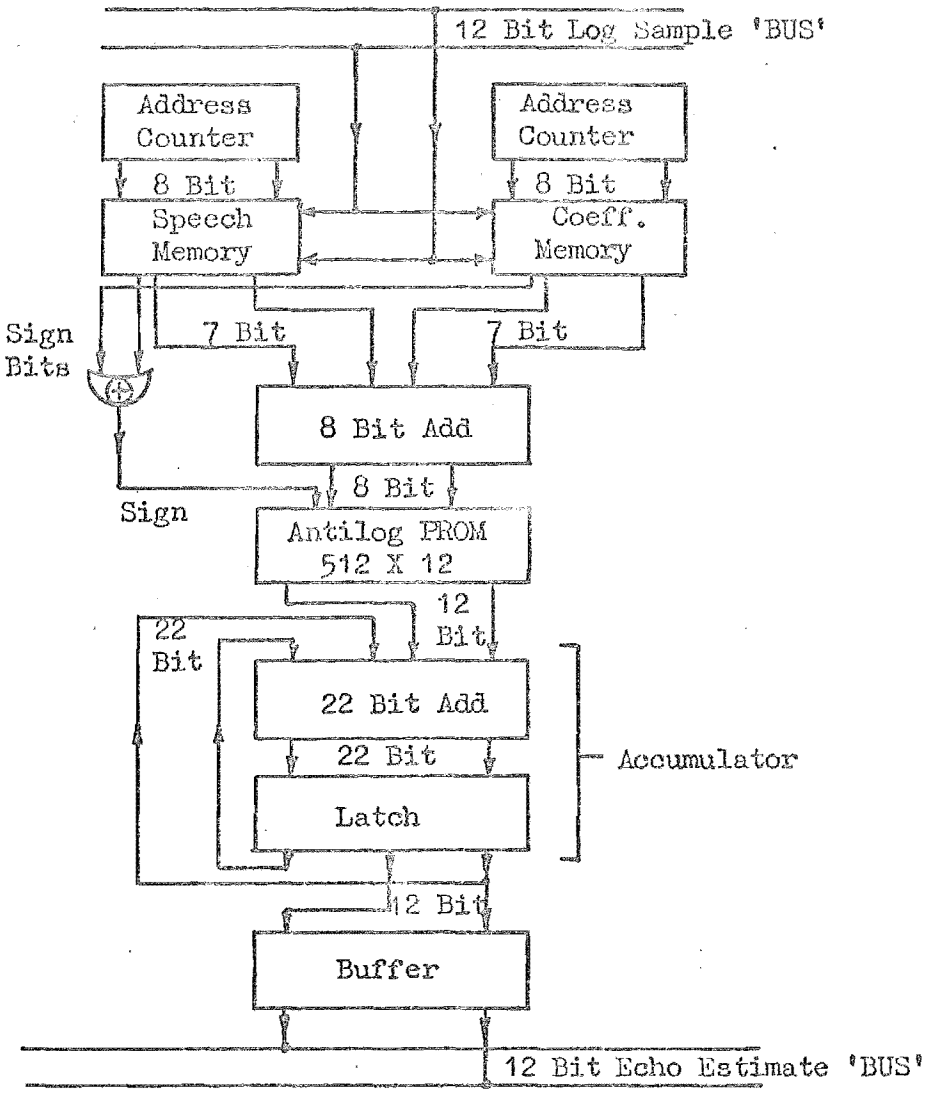


Fig. A5.11. Block diagram of Convolution Circuitry

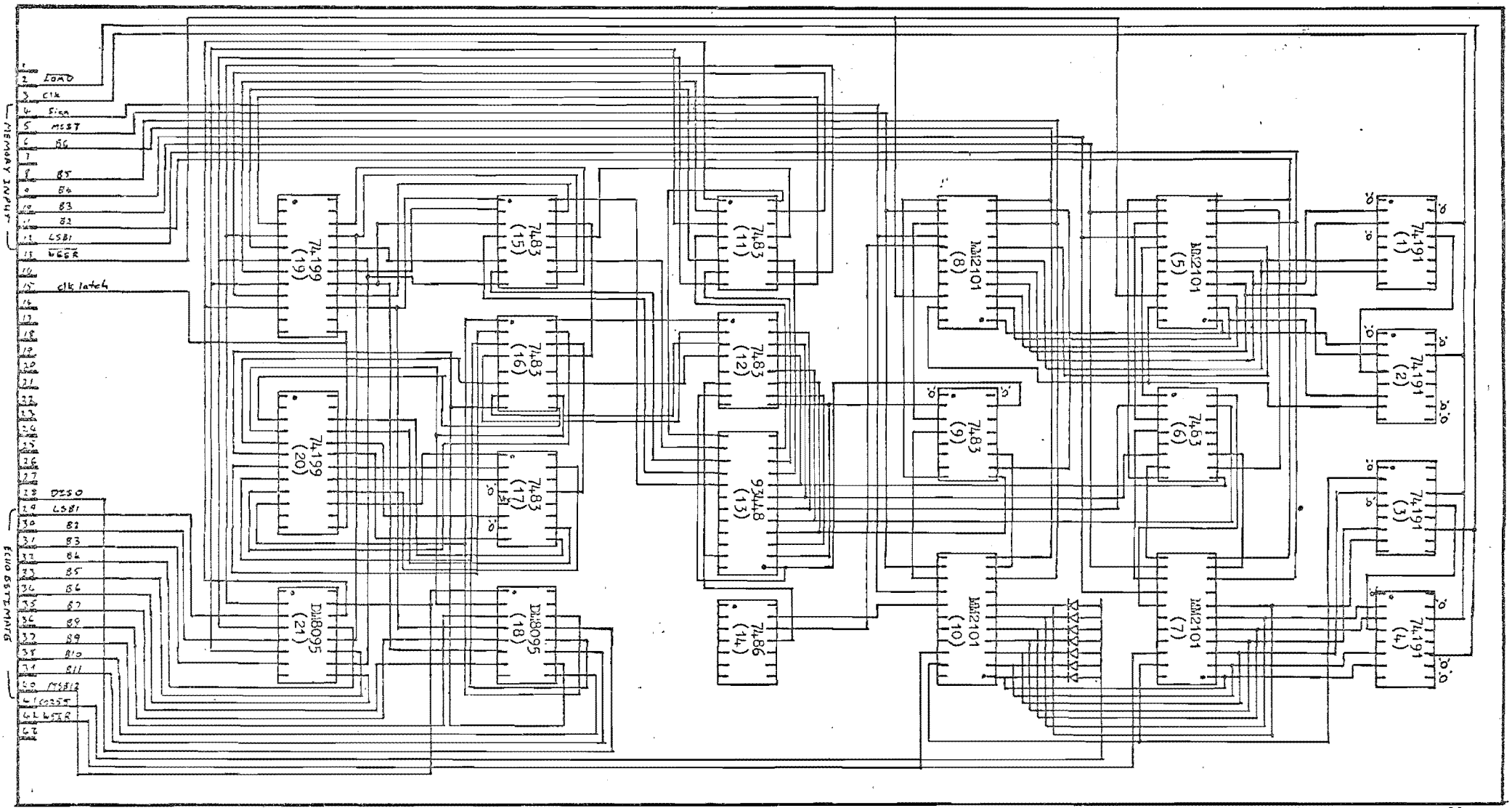


Fig. A5.12. Convolution Board Circuitry

calibration cycle according to the signal $\overline{WEIR}$ generated from the channel write enable timing $\overline{EWT}$ and calibration status signals. Otherwise the speech samples are stored in the signal sample memory (5,8) every 125 uS at the address preceding the previous storage location. The signal RAM address counter (1,2) decrements at an 8 KHz rate. Between the decrements, it increments through 256 at a 2.133 MHz rate to return the counter to the start address. This occurs at the same time as the impulse response counter increments through 256 from zero to zero. The 2.133 incrementing clock is derived from the 6.4 MHz on the logic board. The memories are permanently enabled and the outputs appear assynchronously following a change in the address. The 7 bit magnitude outputs are added (6,9) before being used to address the PROM (13) look-up table. The parity check of the sign bits from memory chooses the true or complement output from the PROM. If the complement output is chosen a '1' is added to the carry input to the adders (11,15,16,17). The result of this is the addition of the two's complement of the magnitude for -ve numbers or a subtraction. The digital accumulator formed by the adders (11,15,16,17) and latches (19,20) is synchronously clocked 1 clock period after the address has changed and as it changes again. The inbuilt delay in the memories, adders and latches prevents a race condition. The digital estimate at the end of the convolution cycle is placed on the 12 bit linear echo estimate 'BUS' through the buffers (18.21).

(d) Logic and Control Circuitry

Refer to Fig. A5.13. This board was designed to provide all the timing required for initial single channel operation.

The 6.4 MHz clock (6) is divided down to give 1.28 MHz (9) for the correlation circuitry and 8 KHz (10,11) for the basic signal sampling timing. The 8 KHz is used to trigger monostable (7A) which provides a 1 uS sample and hold control 'S+H'. It in turn triggers a 200 uS start conversion pulse (7B) 'SCON' for the A/D convertor. It in turn triggers the conversion delay pulse (8A) which finally triggers the write timing pulse '$\overline{\text{EWT}}$' (8B).

The calibration instruction at present is initiated manually on this board and a start calibration pulse (250 uS) 'SCAL' is synchronised to 8 KHz (12A,5A) for the calibration board. The measure period of the calibration cycle is indicated by the output of the Flip-Flop (12B) which is triggered by the 'TRANSMIT' signal from the correlator and cleared when the correlator memory address counter reaches 1280 through gate (2A).

(e) Logarithmic Conversion

Referring to Fig. V.XIV the 12 bit linear samples are converted to sign and magnitude with EXCLUSIVE OR gates (1,2,3) and the magnitude then addresses the PROM look-up table (4,5,6,7) to obtain the logarithm. The output takes the form of a 7 bit logarithm of the magnitude and a separate sign bit.

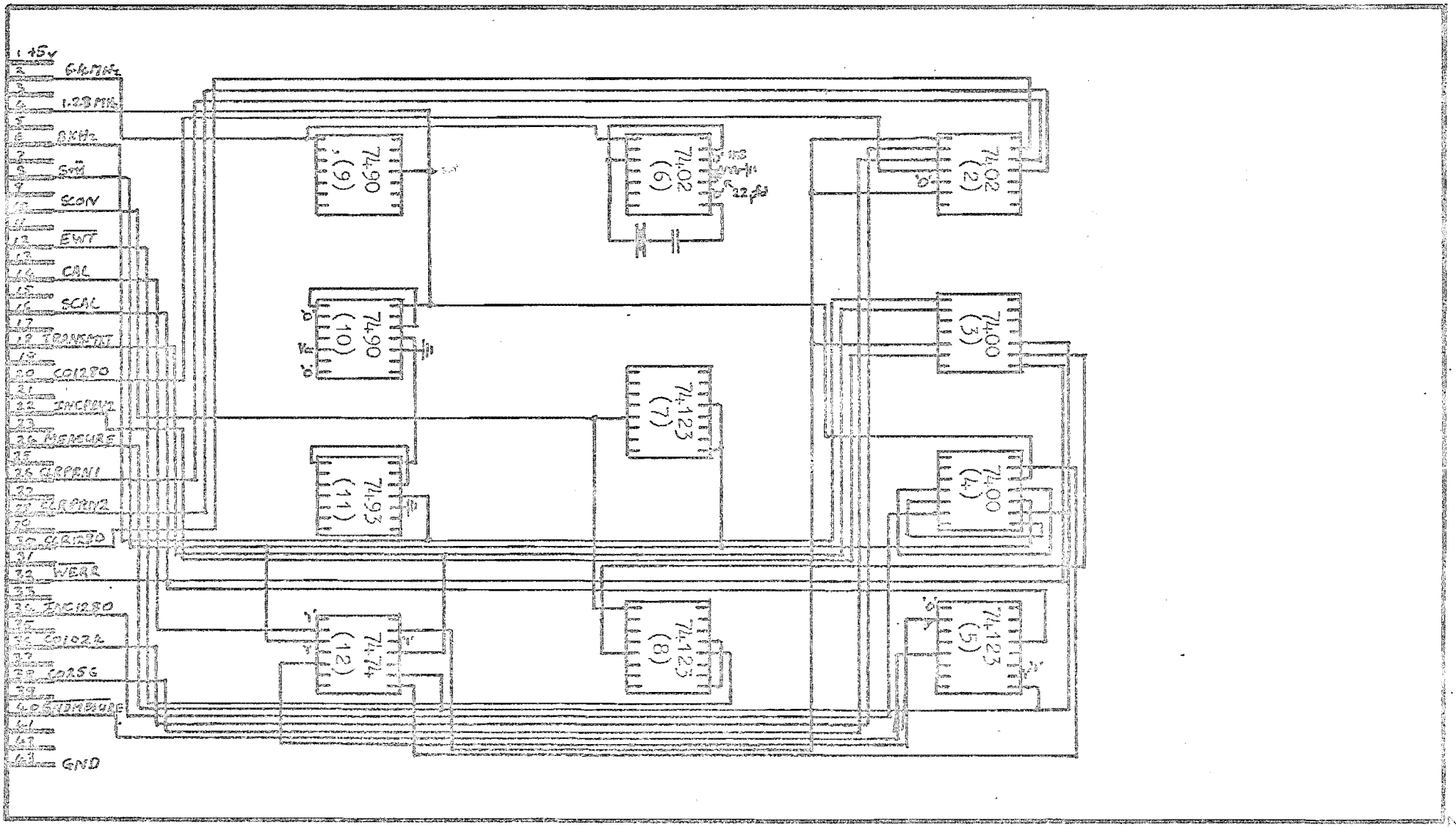


Fig. A5.13. Single Channel Timing and Control Logic (supplement to original design)

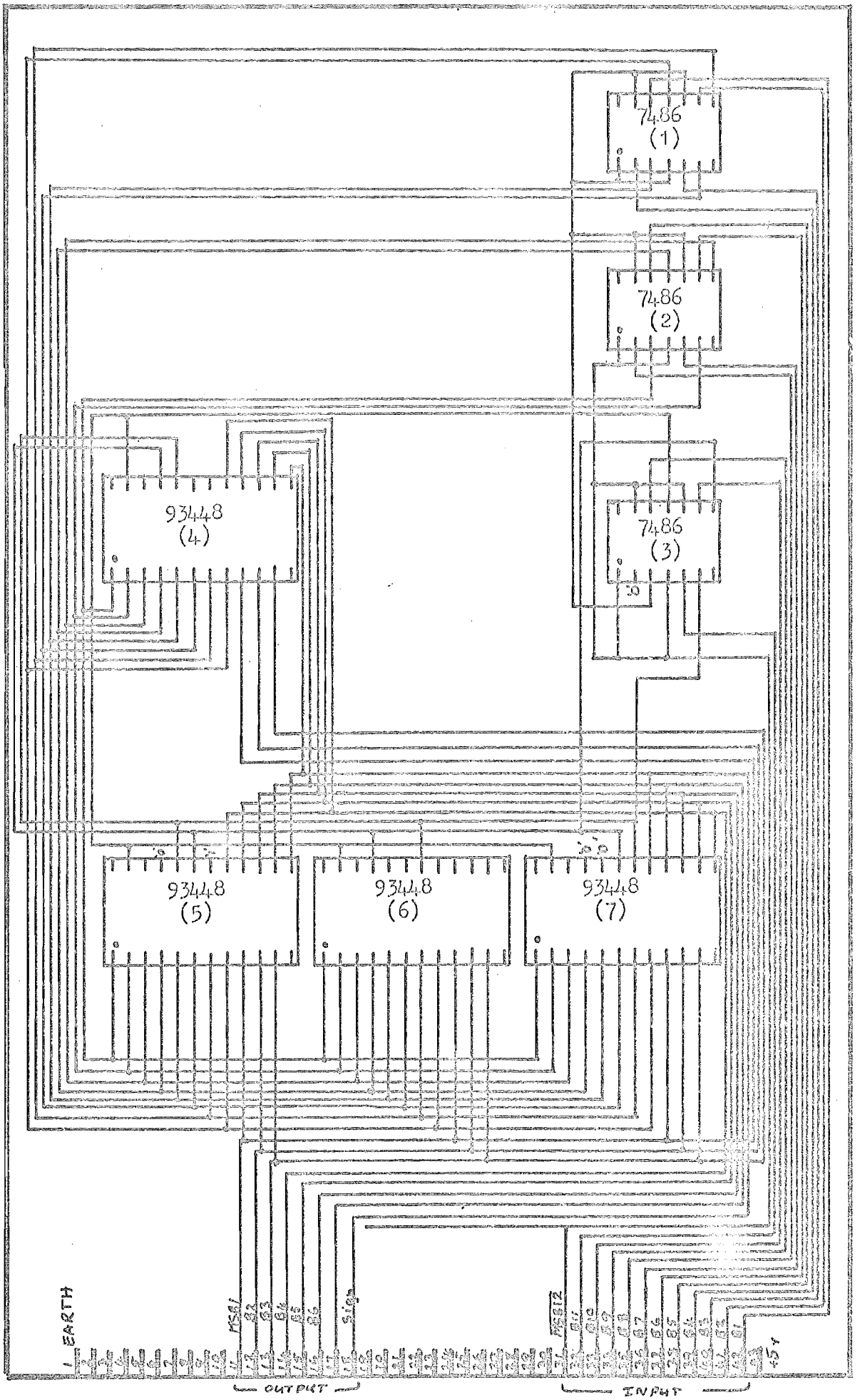


Fig. A5.14. Logarithmic Conversion Circuitry

APPENDIX VI

CROSS CORRELATION CHECK OF CANCELLER PERFORMANCE

As the echo path model is a discrete time system this process will also be considered a discrete time operation. A diagram showing the signal components present in this operation is given in Fig. A6.1.

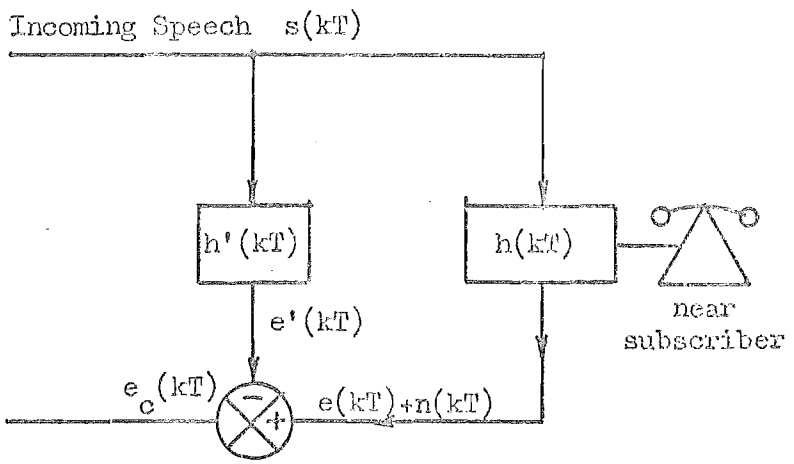


Fig. A6.1 Components Present at Point of Cancellation

A description of these components is as follows:

h(kT) is the discrete impulse response of the echo path.

h'(kT) is the impulse response of the echo path model.

e(kT) is the true echo.

e'(kT) is the estimate of the echo.

n(kT) is the system noise including speech from the near subscriber.

Now system noise is defined as being any component not present at the point of incoming speech and consequently not operated on by the canceller. This noise can, therefore, include speech from the near end subscriber at a level of -17 dBmO.

Now a measure of canceller performance is the degree to which e'(kT) matches e(kT). If e'(kT) is not cancelled by e(kT) some portion of e'(kT) will appear at $e_c(kT)$. Now by cross correlating e'(kT) and $e_c(kT)$ a measure of the level of e'(kT) present in $e_c(kT)$ will result.

$$\text{Now } e_c(kT) = e(kT) + n(kT) - e'(kT)$$

To avoid instability around the 4 Wire transmission path a margin of 2 dB for echo transfer attentuation is an accepted minimum in New Zealand. This means that the R.M.S. value of the echo will be lower than - 19 dBmO whereas the R.M.S. value of n(kT) due to active speech will have a maximum of - 17 dBmO. As the noise is statistically independent of e'(kT) the cross correlation of $e_c(kT)$ and e'(kT) will be zero if e'(kT) = e(kT) and the correlation is over an infinite time period. This cross correlation is given by;

$$\Psi_{e'c}(kT) = \sum_{i=0}^{i=\infty} e'(k+i)e_c(iT)$$

$$= 0 \text{ for } e'(kT) = e(kT)$$

However, if this average is limited to say 'I' samples of i;

$$\Psi_{e'c}(kT) \neq 0 \text{ even for } e'(kT) = e(kT) \text{ unless}$$
$$n(kT) = 0 .$$

Some expected upper limit can be estimated, however, as this represents the product of two instantaneous amplitude distributions. Now n(kT) has a maximum σ (rms or standard deviation) of - 17 dBmO and a mean of zero. The echo estimate has a similar instantaneous amplitude distribution with a mean of zero and a maximum σ of - 19 dBmO. The product of these two distributions will have a mean of zero and a maximum σ (rms or standard deviation) of (-17 - 19) dBmO, i.e. - 36 dBmO.

After initial calibration any time variance can be expected to vary the amplitude and phase of the echo but not the time delay around the echo path. This cross correlation check can, therefore, be limited to time k = 0. The cross correlation resulting from this limitation is defined here to be a single point correlation and is represented by;

$$\Psi_{e'c}(OT) = \sum_{i=0}^{i=I} e'(iT)e_c(iT)$$

$$= \sum_{i=0}^{i=I} e'(iT)(e(iT) - e'(iT) + n(iT))$$

$$= -\sum_{i=0}^{i=I} (e'(iT))^2 - \sum_{i=0}^{i=I} e'(iT)e(iT) - \sum_{i=0}^{i=I} e'(iT)n(iT)$$

dividing through by $-\sum(e'(iT))^2$

$$\Psi_{e'c}(OT) = 1 - \frac{\sum_{i=0}^{i=I} e'(iT)e(iT)}{\sum_{i=0}^{i=I} (e'(iT))^2} - \frac{\sum_{i=0}^{i=I} e'(iT)n(iT)}{\sum_{i=0}^{i=I} (e'(iT))^2}$$

goes to zero for

accurate cancellation

Now e'(iT) and n(iT) have similar amplitude distributions with standard deviations $\sigma_{e'} = .11$ and $\sigma_n = .14$ respectively.

$\sum_{i=0}^{i=I} e'(iT)n(iT)$ therefore has distribution with

$$\sigma_{e'n} = .14 \times .11 = .016$$

The sum of 'I' samples will, therefore, have an R.M.S. value of .016

The standard deviation of $\sum_{i=0}^{i=I} (e'(iT))^2$ is;

$$\sigma_{e'e'} = .11^2 = .012$$

The sum of 'I' samples being I x $\sigma_{e'e'}$ = .012 x I

The amplitude of the noise component in this correlation is, therefore;

$$.016/(.012xI)$$

$$\text{or } 1.33/I$$

The required measure of the accuracy of cancellation is taken from the term;

$$1 - \frac{e'(iT)e(iT)}{(e'(iT))^2}$$

The closer e'(iT) represents e(iT) the closer this term approaches zero. The amplitude of this term will vary both with amplitude and phase variations of e'(iT). An accurate estimate of the amplitude of this term for a given inaccuracy of the echo path model will depend on the type of time variance - whether it be phase or amplitude or both. Some idea of the magnitude of this term can be gain however. If the amplitude of the true echo increases by 10% (.83 dB) the amplitude of this error term becomes (1 - 1.1) which has a magnitude of 0.1. When the magnitude of this is compared with that of the noise term (1.33/I) it is clear that this would give a reliable indication of inaccurate cancellation for I greater than 100. A change in echo level of this magnitude represents 90% cancellation corresponding to an echo return loss enhancement of 20 dB. Longer time constants would give proportionately more accurate indications

but would be slower to recognise the error. 100 samples represents a delay of only 12.5 mS so an average over 1000 sample periods or 125 mS would be more suitable.